The Bias-stress Effect in Pentacene Organic Thin-film Transistors

by

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Submitted to the Department of Electrical Engineering and Computer Science
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Abstract

Organic thin-film transistors (OTFTs) are promising for flexible large-area electronics. However, the bias-stress effect (BSE) in OTFTs causes operational instability that limits the usefulness of the OTFT technology in a wide range of circuit applications. Currently, most existing studies on OTFT BSE are inadequate because of one or more of the following reasons. First, they study the BSE on OTFTs with thermally grown SiO_2, which cannot be used in flexible electronics due to its high deposition temperature. Secondly, they use devices with no encapsulation, and the devices degrade by exposure to H_2O and O_2 in ambient air. The existence of such other degradation mechanisms complicates the interpretation of the BSE measurements on these devices. Lastly, they do not study the BSE systematically to fully identify its dependencies on various stress conditions. This work addresses these issues by systematically studying the electrical characteristics of the BSE in integrated pentacene OTFTs with polymer gate dielectric and encapsulation. Pentacene is used as the model organic semiconductor because it is the most widely used organic semiconductor for OTFTs.

The measurements reveal that the BSE results from carriers that are trapped at the semiconductor/dielectric interface. The BSE can be accurately modeled by a shift in the gate voltage, ΔV, which equals qN/C_i, where N is the density of trapped carriers, and C_i is the channel capacitance per unit area. The BSE occurs only when both gate field and channel carriers are present and the drain current does not increase the BSE. Because the density of traps is limited, when there are more carriers induced in the channel than available number of traps, ΔV saturates at a constant value, which is directly proportional to the trap density in the channel. This behavior of ΔV saturation despite the presence of free carriers in the channel is observed for the first time in a TFT.

Through the temperature measurements, we identify that the source of the long time constants for trapping is the high energy barriers for carriers to be trapped. The effective energy barrier is found to be 0.8 eV for the measured pentacene OTFTs. The time constants associated with the traps are dispersed due to the disorder in the pentacene and gate dielectric. The dependencies of the BSE to various stress conditions are modeled, which allows prediction of ΔV for different stress times and voltages. The model is used to estimate the implication of the BSE on circuit applications and usable lifetime.

Full recovery of the original I-V characteristics occur when the bias stress is removed. The recovery is found to have time dependency and thermal activation energy that is similar to the BSE implying that the recovery mechanism is similar to that of the BSE. The application of the negative V_{SG} accelerates recovery, which serves as evidence that the recovery is achieved by detrapping of the trapped carrier. Possible mechanisms for the BSE and its recovery are discussed based on the experimental observations.

A new annealing process which improves mobility, contact resistance, and operational stability has been developed. Experimentally the annealing process increased mobility from 0.03 to 0.05 cm^2/Vs and decreased contact resistance from 185 to 38 KΩ-cm. The overall improvement in stability is over eight times for a wide range of stress conditions. The stability is found to be increased by the reduction of the trap density and the decrease of the trapping rate.

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Title: Professor, LeBel Chair

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Contents

List of Figures

List of Tables

Chapter 1

Introduction

Organic thin-film transistors (OTFTs) that use organic semiconductors as the active layer are promising for large-area flexible electronics. Once only an academic research topic because of their low mobility, they now have sufficient electronic performance for many applications. For example, flexible backplanes for OLED and LCD displays and new electronic Braille sheets have been demonstrated with OTFTs [1,2,3]. In addition, they can be deposited from solutions, which makes them compatible with low-cost manufacturing methods such as roll-to-roll processing. Companies such as Plastic Logic and PolyIC are preparing to launch the first commercial applications based on solution processed organic transistors [4,5].

Thin-film transistors (TFTs) are a key component in every active-matrix liquid crystal display (AMLCD). Most TFTs currently use thin hydrogenated amorphous silicon (a-Si:H) as the active layer. Due to the disorder in amorphous silicon, a-Si:H TFTs have mobility about a hundred times smaller than traditional single crystalline silicon metal-oxide-semiconductor field effect transistors (MOSFETs). Despite such a drawback, TFTs dominate large-area applications because they can be deposited on large glass substrates, which is not possible with single crystalline silicon MOSFETs due to their high processing temperatures

(> 1000 °C). The state of the art, Generation 10 LCD plants use a-Si:H TFTs on glass substrates that are 2.85 m by 3.05 m [6].

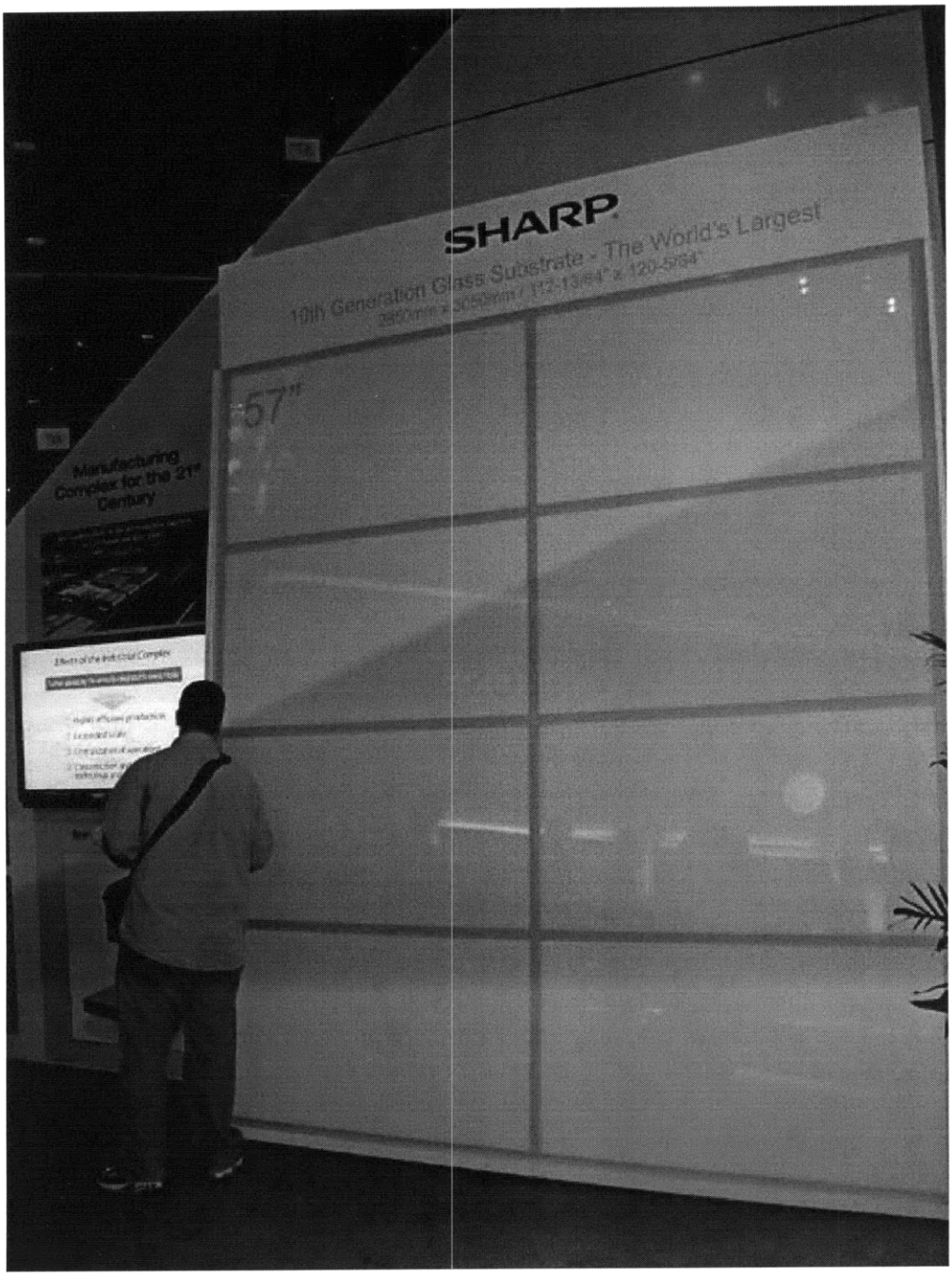

Figure 1-1: Exhibition of Gen 10 (= 2850 x 3050 mm) glass for AMLCDs.

TFT technology has found a niche in LCDs where the performance requirements are not high and the large area capability is absolutely necessary. Initially, passive-matrix LCDs were most widespread because of their simplicity. However, passive-matrix LCDs are limited in size due to the leakage current and noise characteristics in the liquid crystals (LCs) [7]. In AMLCDs, TFTs are used as switches to access the individual pixels and reduce parasitic leakage current through the LCs by orders of magnitude so that more columns can be driven in a display. Also, they increase the yield of the completed display because a single short in a pixel does not result in the entire column being shorted as it does in passive-matrix LCDs. The ability to drive more rows and increase yield made TFTs critical in large, high information density LCDs — an industry that has grown to a $30 billion-a-year business [8]. The dominant TFT technology used in AMLCD today is a-Si:H TFT technology.

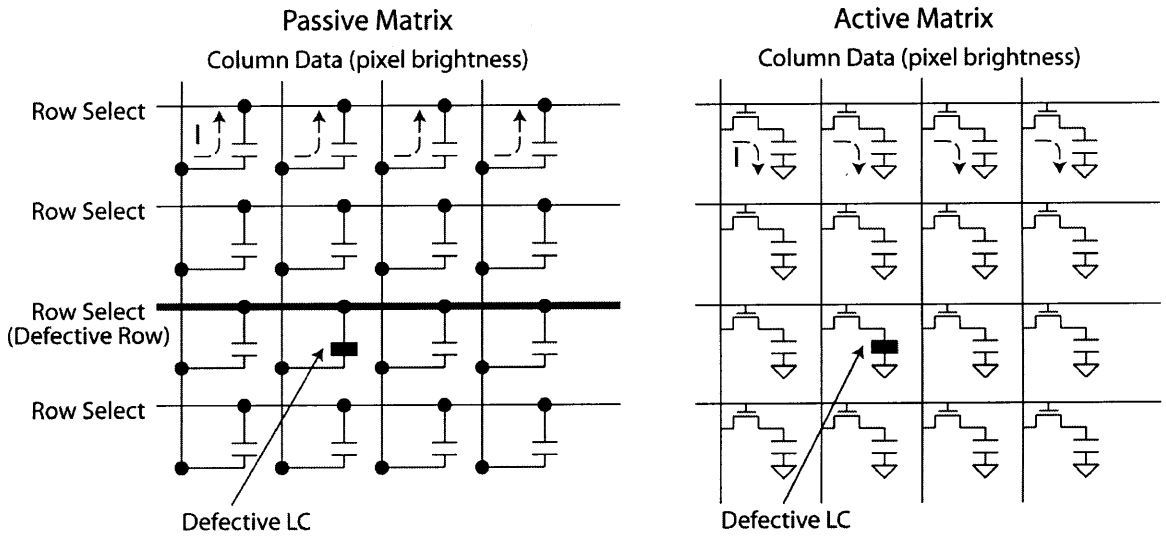

Figure 1-2: Passive-matrix vs. active-matrix backplane. In passive-matrix configuration, the LC leaks current from data line to the row select line. The total leakage current to the row select line increases with number of columns and limits the number of columns. In active-matrix configuration, there is no such limit because the leakage current is controlled by a TFT. Also in a passive-matrix backplane, a defective LC results in the whole row being defective whereas in active-matrix, a defective LC only affects a single pixel.

1.1 **Problem Statement**

With the maturing LCD industry, interest has risen in using TFTs for new flexible large-area electronics which are made on plastic substrates. Plastic substrates can be used to make light-weight rugged displays which are easy to transport and do not shatter. Large rugged displays which can be rolled up to fit in a pocket have been envisioned for mobile and military applications as shown in Figure 1-3. Other applications such as imagers with curved surface to relax requirements on lens design [9] and flexible sensors which can sense temperature and pressure over large area have been proposed for robotic skins [10].

There are a number of requirements that must be met in order to realize flexible electronics on plastic substrates. First of all, the device must be flexible. Single crystalline devices cannot be bent because bending them will typically shatter them. Secondly, the processing temperature must be low or a thermal barrier layer must be developed so that the underlying plastic substrate is not degraded. If the processing temperature is kept below 150 °C a number of electronic-grade plastic substrates can be used as shown in Figure 1-4 [11].

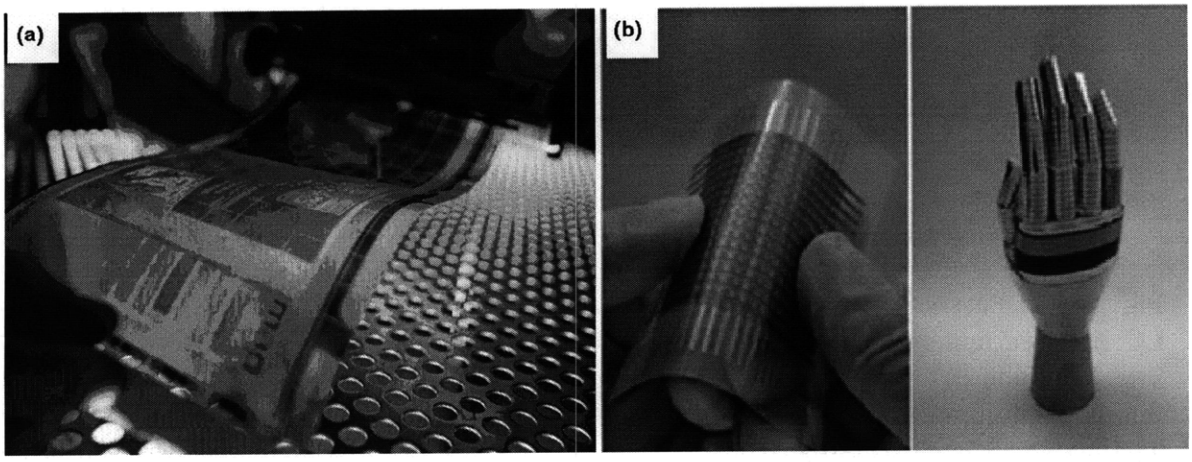

Figure 1-3: (a) A concept of rollable display for mobile applications. Courtesy of Phillip Spears and HP. (b) Flexible temperature and pressure sensors for robotic skins [7].

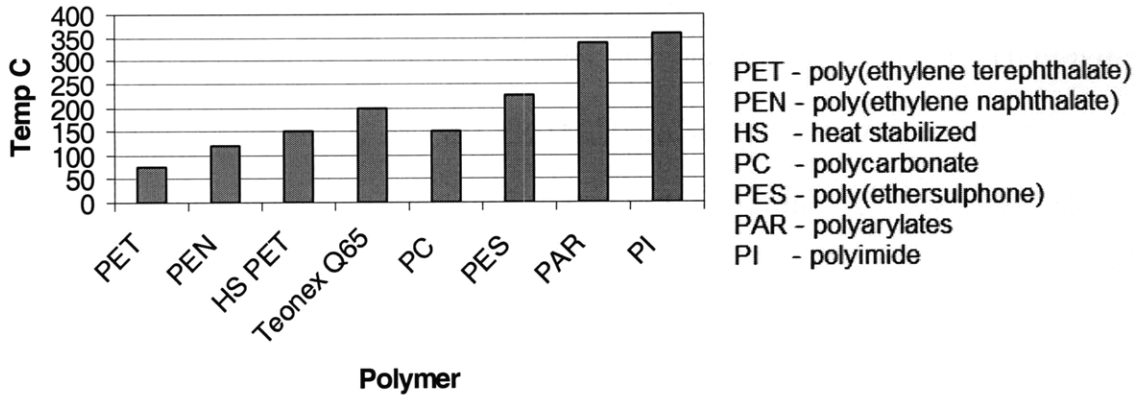

Figure 1-4: Glass transition temperature of electronic-grade plastic substrates [11]

Conventional a-Si:H TFTs do not meet this requirement as they require processing temperatures typically around 200-300 ^{o}C [12]. Lastly, there are other requirements relating to the manufacturing cost and yield that need to be met for practical applications.

Organic TFTs meet all these requirements for flexible electronics. Recently, Sekitani and Someya have fabricated OTFTs with mobility of 0.58 cm^2/Vs and on/off ratio of 10^5 on flexible polyimide (PI) films [13]. They demonstrate that these transistors exhibit only 4% change in mobility when rolled to a radius of 2 mm and can be stored in air without much degradation if proper encapsulation is applied.

However, OTFTs exhibit the bias-stress effect (BSE) which causes operational instability that limits them from being used in a wide range of circuit applications. The BSE refers to the change in characteristics of the transistors due to application of electric bias stress. The BSE causes drain current degradation in TFTs which leads to circuit failures that limit the lifetime of the circuit. For any applications that use OTFTs as analog circuit elements, the

BSE needs to be addressed. One example is the backplane for organic light-emitting-diode (OLED) displays. OLED technology is the next generation display technology that consumes less power, has more vibrant color, higher contrast, and simpler device structure than LCDs [14]. However, in contrast to LCDs, OLEDs require constant current to drive them. Therefore the transistors are used as constant current sources. The change in TFT characteristics results in direct degradation of the picture quality, and thus more stable TFTs or a compensation scheme for the BSE needs to be considered [15]. For practical usage in a wide array of applications, the BSE needs to be reduced.

This work aims to develop a methodology to characterize the BSE in OTFTs and characterize it with respect to various stress conditions and investigate the cause of the BSE in pentacene OTFTs by means of electrical characterization methods. Pentacene is chosen as the model organic semiconductor because it is the most widely studied organic semiconductor for OTFTs owing to its high mobility and robustness. The effect BSE has on circuit lifetimes is studied, and careful measurements are taken to identify the physical source of the BSE. Afterwards, a method to reduce the BSE is developed, and the cause of the improved stability is investigated.

1.2 Structure of Thesis

The thesis is structured as follows. We begin by introducing the basic theory of operation of OTFTs in Chapter 2. In Chapter 3, the process for integrated pentacene OTFTs developed at MIT is described in detail. The process has been used to prepare samples measured in this

work. We underline the key decisions leading to the use of various processes and physical characteristics of the dielectric and the semiconductor. Chapter 4 then discusses key characterization methods in OTFTs. In Chapter 5 we characterize the BSE in OTFTs with the use of the characterization methods introduced in Chapter 4 for various parameters. We investigate the dependence on channel length, temperature, and bias voltage during stress and discuss the implications of these results to circuit lifetime. Chapter 6 measures the recovery from the BSE after the bias stress is removed. Chapter 7 introduces a new annealing procedure that reduces the BSE. A series of measurements is performed to identify the source of the reduced BSE. Finally, Chapter 8 summarizes the accomplishments of this work and contains suggestions for future work.

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Chapter 2

Introduction to OTFTs

Organic semiconductors have been studied as early as the late 1940s [1]. In 1948, Eley and Vartanyan have reported experimental studies of dark conductivity in phthalocyanines. Beginning in 1980s, organic TFTs based on polymer and small molecule semiconductors have been studied. However the performance of these devices was poor and the interest in OTFTs remained largely an academic curiosity. Through the research of better materials and device structures, OTFTs with mobility surpassing that of a-Si:H have been demonstrated in the late 1990s [2]. Figure 2-1 shows the progress of the largest reported mobility from 1986 to 2006. The performance of small molecule organic semiconductors is better than that of polymer semiconductors, and both have shown impressive progress in the last two decades.

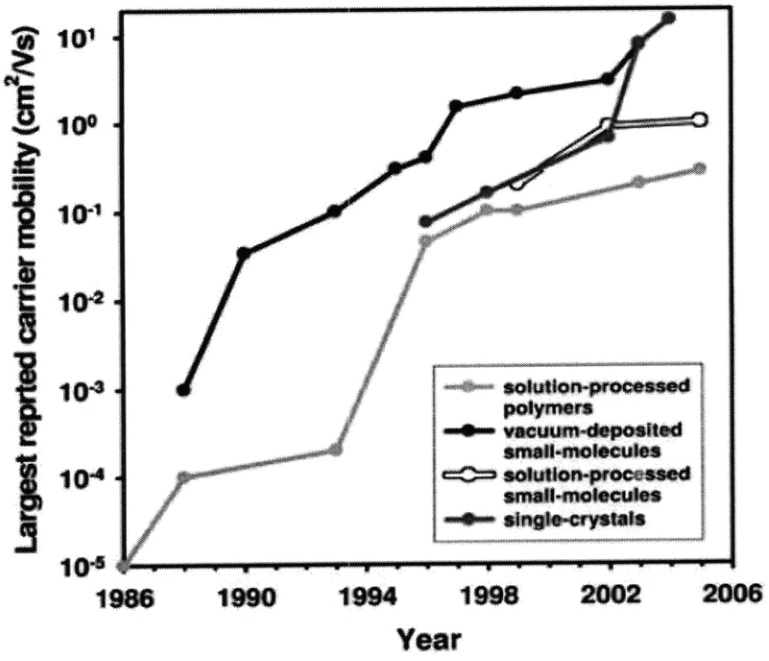


Figure 2-1: Improvement of mobility in organic semiconductor over the years. Rates of mobility increase have been similar for single crystals, polymers and small molecules. [3]

The research result of OTFTs with comparable performance to a-Si:H TFTs generated great interest in both academia and industry because organic semiconductors had several key advantages compared to amorphous silicon. First, the substrate can be at room temperature during the deposition step as organic semiconductors can be evaporated at low temperatures owing to their van der Waal bonds which are substantially weaker than covalent bonds. This low temperature deposition opened up the exciting possibility of integrating electronics on surfaces that were not available for electronics before. A number of groups have demonstrated functional transistors on various flexible substrates including plastics [4] and even on paper [5].

Secondly, various physical properties such as the band gap and surface affinity of organic semiconductors can be controlled with the synthesis of new organic semiconductors. Such controllability can be used to make organic semiconductors that emit different colors of light for OLEDs and semiconductors that respond selectively to chemicals for sensing chemicals. In addition, this controllability allows the use of molecular self-assembly to enable highly ordered films without the need to anneal or increase deposition temperatures. This controllability is possible because larger molecular building blocks are used instead of atoms.

Thirdly, organic semiconductors can be deposited via solution processing. The solution deposition process allows OTFTs to be printed using conventional low-cost patterning methods in a roll-to-roll fashion akin to printing newspapers. The solution processing methods are envisioned to lower the manufacturing cost of electronics per area. Although solution processing has been performed mostly with polymer semiconductors, many groups have shown small molecule organic semiconductors can be also deposited via solution process by modifying the side groups to tune the solubility of organic semiconductors. Moreover, recent research has shown that even small molecules like pentacene with limited solubility in organic solvent can be used to fabricate high performance ($\mu > 0.5$ cm^2/Vs) OTFTs from solution deposition [6]. These three key advantages of room temperature deposition, tunable semiconductor properties, and low cost patterning methods provide exciting research opportunities for OTFTs.

2.1 Structure of OTFTs

OTFTs consist of at least five different layers. The substrate provides mechanical support as the thickness of the individual films is typically less than a micron each. Additionally, there are the gate, dielectric, source-drain, and semiconductor layers. The gate layer is separated from the semiconductor layer by the dielectric, whereas the source-drain layer is in direct contact with the semiconductor. The contact is necessary to inject and extract carriers from the semiconductor. Some common OTFT structures are shown in Figure 2-2. Depending on the location of the gate and the semiconductor with respect to the substrate, the transistor is categorized into bottom gate (inverted) or top gate (non-inverted) structure. The inverted terminology comes from the fact that the gate is at the bottom, contrary to traditional silicon MOSFETs. Most OTFTs are in bottom gate configuration because organic semiconductors can be easily damaged from processing, and this configuration minimizes processing steps for the organic semiconductors. In addition, depending on the location of the contact with respect to the semiconductor, the transistor is further categorized into bottom contact (coplanar) or top contact (staggered). In OTFTs, a top contact (TC) structure has been reported to have lower contact resistance perhaps due to the penetration of metal dopants into the semiconductor resulting in doped semiconductor contact [7]. However the top contacts can only be deposited through shadow masks which limit the resolution to about 50 μm. Bottom contact (BC) configuration allows the use of conventional photolithographic patterning technique which allows submicron channel-length OTFTs. Photolithographic patterning technique is also the proven scalable large-area technology used for commercial AMLCDs.

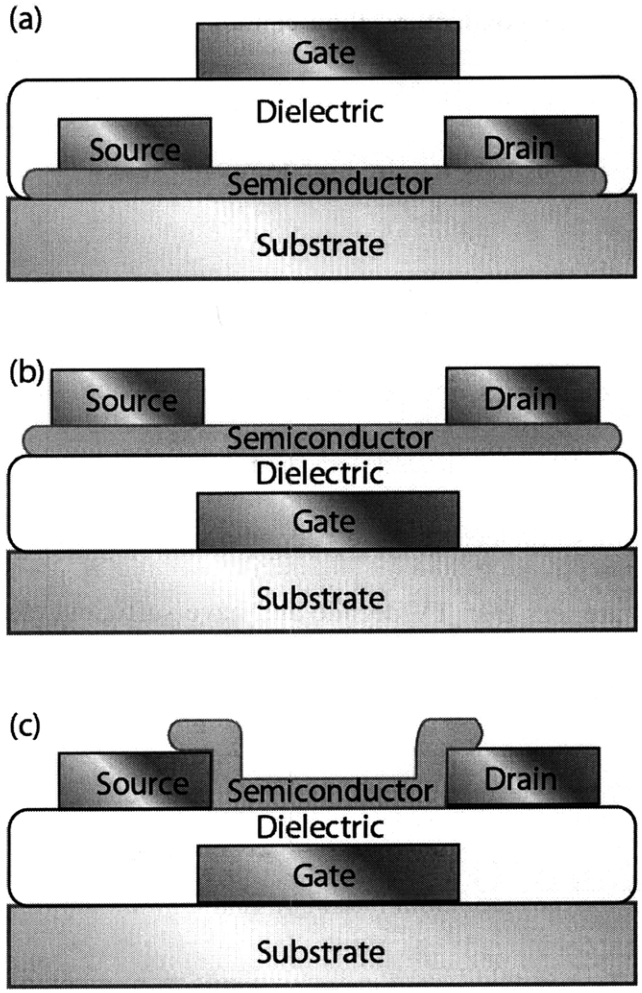


Figure 2-2: Common OTFT structures. (a) Top gate, top contact. (b) Bottom gate, top contact. (c) Bottom gate, bottom contact configuration.

In many works, heavily doped silicon wafer is used as the gate layer because it provides an accessible method of fabricating OTFTs. Silicon wafers are commercially available with thermally grown silicon dioxide which can be used as the gate dielectric. Therefore, the use of silicon wafer only requires the growth and patterning of two additional layers to complete the OTFTs. The widely available silane surface treatment for silicon dioxide is also a notable advantage of using heavily doped silicon and silicon dioxide systems. Many research works continue to use silicon substrates with the aim of investigating and improving organic

semiconductor properties [8]. Although such devices serve the need for preliminary research work for new organic semiconductors, they cannot have patterned gates crucial for circuit applications. In addition, the use of thermally grown oxide in flexible or large area electronics is not possible as they require high temperature.

Recent works have started employing different dielectrics that can be deposited at low temperatures. Such dielectrics include spun cast polymers like polyimide [9], CVD evaporated polymers [10], self assembled monolayer [11], and organic/inorganic hybrid dielectrics [12]. All these dielectrics have been shown to have low interface states such that subthreshold slopes are less than 1V/decade and have sufficient electrical performance with mobility > 0.1 cm^2/Vs.

2.2 **Fabrication of OTFTs**

Fabrication of OTFTs has been demonstrated using a number of techniques [8]. Among many techniques, additive printing methods that are compatible with roll-to-roll fabrication are notable as these methods enable low-cost electronics on large-area flexible substrates. OTFTs with all the layers printed via additive processes have been demonstrated [13]. Additive processes are advantageous compared to subtractive processes because they are simple and have higher material utilization. In a subtractive patterning process, a photoresist must be patterned to the substrate, the patterned layer must be etched, and finally the photoresist layer must be removed to complete the process. An additive process reduces all these steps into a single step, which represents significant savings on cost. Because superior

resolution offered by lithographic patterning is not required for low performance electronics over large area, the printing process is preferred for low-cost large-area applications. There are a number of additive processes available for organic semiconductors in traditional graphical printing methods such as flexography, gravure, offset, and inkjet. Subramanian *et al.* have demonstrated a subset of these printing methods for printing electrodes on flexible surfaces [14]. The table below shows the comparison of various printing methods.

Printing technique	Layer thickness (μm)	Feature size (μm)	Viscosity (mPas)	Throughput ($m^2 s^{-1}$)	Registration (μm)	Features/ issues	Examples of graphic art applications
Letterpress	0.5–1.5	>50	50000–150000	1	<200		Books
Flexography	0.8–2.5	80	50–500	10	<200	Wide range of substrates, medium quality	Packaging; newspaper; labels
Gravure	0.8–8	75	50–200	60	>10	Large run length; high quality	Magazines; plastic film and metal foils; bank notes
Pad	1–2	20	>50	0.1	>10	Nonplanar objects	Toys; CDs; pens
Offset	0.5–1.5	10–50	40000–100000	5–30	>10	High quality; need for ink additives	Newspapers; magazines; books
Screen	30–100	20–100	500–50000	2–3	>25	Wide range of inks; medium quality	Textiles; PCBs; CDs; large posters
Inkjet	<0.5	20–50	1–30	0.01–0.5	5–20	Digital data; local registration	Desktop; variable data

Table 2-1: Features of different large-area compatible patterning methods. From [15].

Although these new patterning methods are promising, they are not production-ready in terms of yield and reproducibility and need to be improved. Photolithography has been the standard method of fabrication in microelectronics and in large-area electronics with high yields and reproducibility. High yields are necessary to make circuit applications, so the lithographic process is used in this work to study electrical characteristics of OTFTs. The specific process to fabricate OTFTs will be introduced in the next chapter.

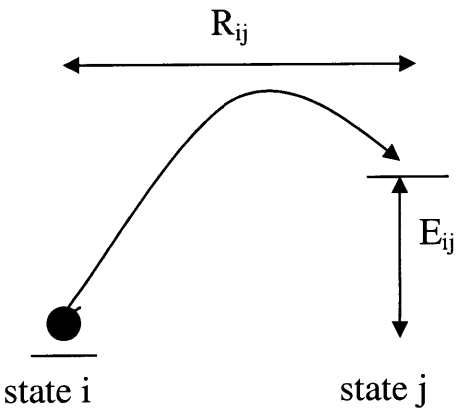
2.3 Transport in Organic Semiconductors

Transport in organic semiconductor is a topic of much debate. It has been observed that mobility in OTFTs increases as the field and temperature increase. It has been theorized that in organic single crystals the transport is dominated by hopping [16]. The van der Waal bonds that hold organic molecules together are on the order of 0.1 eV in contrast to 1 eV of covalent bonds resulting in weak interactions of electron wave functions from adjacent molecules. As a result, the carriers are bounded and localized on a molecule which results in hopping transport. The hopping rate increases with field and temperature as the carriers can hop from one state to another state easily in the presence of field and at higher temperatures. The hopping rate from state i to j can be generally expressed as the following [17]:

$$\begin{aligned} r_{ij} &= \nu_0 \exp(-E_{ij}/kT)\exp(-2\gamma R_{ij}) \qquad \text{if } Ej > Ei \\ r_{ij} &= \nu_0 \exp(-2\gamma R_{ij}) \qquad \text{if } Ej < Ei \end{aligned} \tag{2-1}$$

where r_{ij} is the hopping rate, ν_0 is the attempt frequency, $E_{ij} = E_j - E_i$, E_i and E_j is the energy of states i and j respectively, R_{ij} is the distance between states i and j, and γ^{-1} is the decay

length of the wave functions. Naturally, the hopping transport in organic crystals leads to temperature and field dependence in amorphous and polycrystalline organic semiconductors as well.



hopping rate:

$$\nu_{ij} = \nu_0 \exp(-2\gamma R_{ij}) \exp(-E_{ij}/kT)$$

Figure 2-3: Hopping rate between two states.

However, experimental measurements on different organic single crystals such as naphtlaene, rubrene, and pentacene have been reported to have band transport-like behavior where the mobility decreased as the temperature increased, and the mobility is independent of the gate field [18]. In band transport, mobility decreases as temperature increases because of the increased phonon scattering. Likewise, the field would not have a strong effect on mobility if the carriers are delocalized in extended states. This indicates that transport in organic single crystals may be band transport despite the weak van der Waal bonds between the molecules.

In OTFTs which use disordered film of organic semiconductors, we observe increasing mobility with temperature and field in contrast to what is observed for single crystalline organic transistors. The transport in these disordered materials can be explained with band transport in the framework of trap limited conduction (TLC) model. In TLC model, most of

the induced carriers in the channel are not mobile, and charge transport is dominated by a small number of carriers that are at a relatively high mobility states. Such states can be the extended states where carriers are free to move around. For convenience, the states with high mobility will be referred to as the free states, and the energy at the free states will be denoted as E_V, to make the terminology consistent with the existing silicon literatures. The term E_V is used interchangeably with highest occupied molecular orbital (HOMO) in individual molecules.

In the linear region, the drain current can be expressed as the following:

$$I_D = W\, q\, \mu_{free}\, p_{free}\, E \tag{2-2}$$

where W is the width of the device, q is the charge per electron, μ_{free} is the mobility of the free hole carriers, p_{free} is the density of free carriers, and E is the lateral electric field across the channel. p_{free} is described by:

$$p_{free} = \int_{-\inf}^{E_V} g_V(E)(1 - f(E))dE \tag{2-3}$$

where $g_V(E)$ is the DOS near E_V, and f(E) is the Fermi function. $(1 - f(E))$ is used because carriers are holes. The Fermi function is expressed as the following:

$$f(E) = \frac{1}{1 + \exp(-(E - E_F)/kT)} \tag{2-4}$$

where E_F is the Fermi energy. Because the Fermi energy is above E_V by more than 3kT, Boltzmann approximation can be used for f(E) in Equation (2-3) to yield:

$$p_{free} = N_V \exp(-(E_F - E_V)/kT) \tag{2-5}$$

where N_V is the effective density of free states, defined in a similar manner as in Si MOSFETs. From this relationship, the temperature dependence can be established. The current is proportional to p_{free} which increases proportional to $\exp(-(E_F - E_V)/kT)$. As temperature increases, the term inside the brackets becomes less negative and p_{free} increases exponentially.

The measured mobility of the OTFT can be expressed as [19]:

$$\mu_{OTFT} = \mu_{free} \frac{p_{free}}{p_{induced}} = \mu_{free} \frac{p_{free}}{p_{free} + p_{trapped}} \approx \mu_{free} \frac{p_{free}}{p_{trapped}} \tag{2-6}$$

where μ_{free} is the mobility of the free hole carriers, and p_{free} and $p_{trapped}$ are the densities of free and trapped carriers respectively. The approximation in Equation (2-6) is justified because the density of free carriers is small compared to the density of trapped carriers.

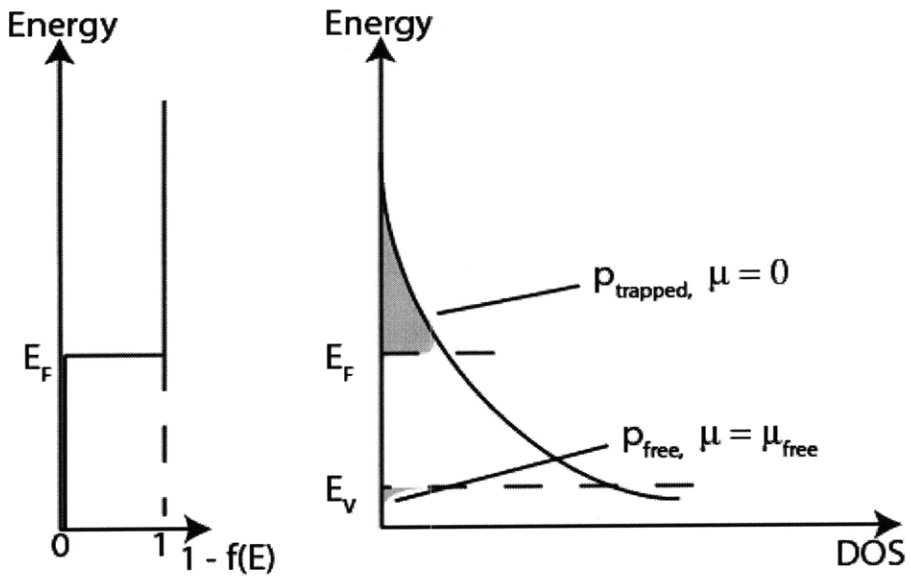


Figure 2-4: Fermi energy level and carrier population at trap states and free states.

$p_{trapped}$ can be expressed as the integration of DOS and the Fermi function:

$$p_{trapped} = \int_{EV}^{inf} g_V(E)(1-f(E))dE \tag{2-7}$$

The integration from infinity may be troublesome, but $g_V(E)$ is usually modeled with a exponential tail states which decreases to 0 as energy is increased, and hence the integration results in a finite number. If the DOS changes gradually with respect to the Fermi function as illustrated in Figure 2-4, the Fermi function can be regarded as a step function where above E_F the states are all filled with trapped holes and below E_F the states are empty. States are modeled as neutral when empty.

$$p_{trapped} = \int_{EF}^{inf} g_V(E)dE \tag{2-8}$$

As the Fermi level moves closer to the E_V with increasing V_{SG}, the $p_{trapped}$ increases with $g_V(E)$ while the p_{free} increases exponentially with $\exp(-(E_F - E_V)/kT)$. Therefore the measured OTFT mobility increases with increasing V_{SG}. Another way to describe what is occurring as the gate voltage increases is that as more charge carriers are induced in the channel they fill the traps so that trapping becomes less efficient and charge transport improves overall.

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Chapter 3

MIT Integrated OTFT Process

This chapter will review the fabrication process for integrated OTFTs developed at MIT used to fabricate the OTFTs studied in this work. The process was carried out using facilities at the Microsystems Technology Laboratories (MTL) in a CMOS compatible class 100 cleanroom. It uses a parylene polymer, which can be deposited on substrates at room temperature, and a pentacene organic semiconductor, which is one of the most widely studied organic semiconductor and has the highest reported mobility in an integrated organic transistor. The process supports up to three metal layers for wiring OTFTs together to make various integrated circuits and systems. The highest processing temperature the substrate is exposed to throughout the process is 95 ^{o}C which is well below the 150 ^{o}C temperature limit that flexible plastic substrates such as PET and PEN can tolerate. Photolithography is used to pattern the various metal and semiconductor layers because it provides high yield and reproducibility. In addition, it is compatible with arbitrary patterns, fine features, and a variety of deposition techniques which allows optimization of material properties.

Generally, pentacene cannot be patterned using photolithographic techniques because organic solvents induce structural change in pentacene which results in poor electrical performance [1]. Several methods have been developed to circumvent this problem. Jackson *et al.* have used water based photoresist to pattern pentacene [2]. Another group has used patterned surface modification layer before the deposition of pentacene [3]. The surface modification layer inhibits ordered pentacene growth on top of it and leads to insulating pentacene layer, thus eliminating the need to pattern the pentacene active layer. I. Kymissis *et al.* [4] have shown that encapsulating pentacene in parylene protects it from the solvents, which enables subsequent patterning using standard photolithography techniques. This method is used here. The process presented in this chapter is similar to the one reported in [5] with some improvements. The noteworthy improvements are described in detail.

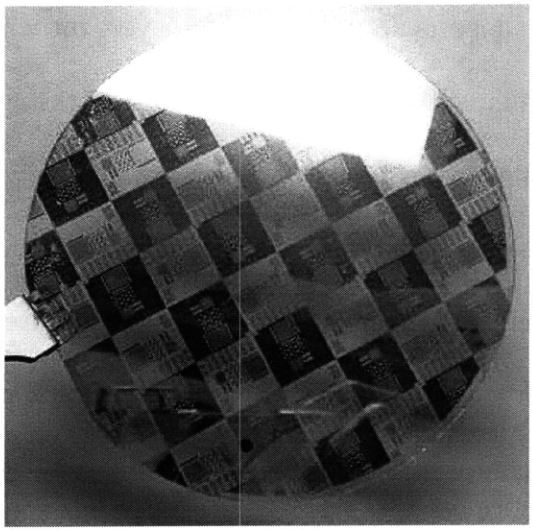

Figure 3-1: A completed wafer of integrated OTFTs.

3.1 Process flow

3.1.1 Gate

OTFTs are fabricated on a 4" wafer-shaped Schott D-263 borosilicate float glass from Erie Scientific. All the processing is done in a class 100 cleanroom and electronic grade chemicals are used to minimize defects due to particles or contamination. The process is illustrated in Figure 3-2. The wafer is first cleaned in a solution of 1:3 hydrogen peroxide and sulfuric acid by volume (Piranha) to clean off organic contaminants and particles generated during scribing. After cleaning, a gate layer consisting of 10 nm chromium and 60 nm gold is e-beam evaporated and patterned. The chromium acts as an adhesion layer for gold. Without it, the gold layer delaminates during subsequent processing. The chromium and gold layers are wet etched by CR-7 etchant (mixture of $(NH_4)_2Ce(NO_3)_6$ and $HClO_4$) and Transene ® Au etchant (mixture of KI and I_2) respectively. The CR-7 has a noticeable undercut and must be timed carefully in order to pattern narrow features. The undercut affects structures that have high aspect ratio severely. For example, structures that are 1000 μm long and 5 μm wide can be undercut completely and stripped away. For this reason, the features on the gate layers are kept above 5 μm and wafers are etched individually to optimize etch time. This limitation in the feature size of the gate layer does not impose a limit on the channel length, which is determined by the feature size of the source/drain layer. After the metal layers are etched, the photoresist layer is removed by commercial photoresist stripper, Microstrip. Microstrip is a mixture of half n-metyl pyrrolidone (NMP) and half 20(20aminoethoxy)ethanol, formulated to strip resist without affecting structural materials.

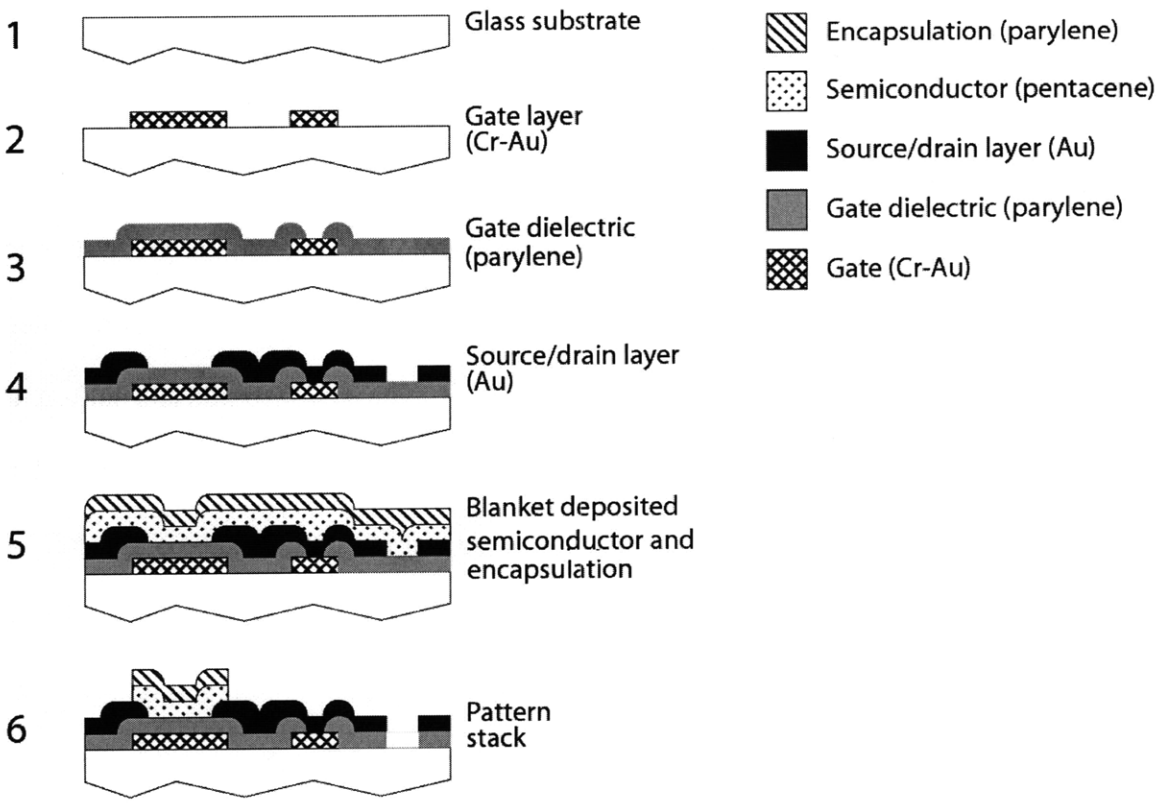

Figure 3-2: MIT process for integrated OTFTs.

3.1.2 Gate Dielectric

Parylene polymer is deposited next as the gate dielectric. Parylene is a trade name of the polymer poly-(para-xylene), which has a chemical formula as shown in Figure 3-3. Parylene is coated on room temperature substrates by hot-filament chemical vapor deposition (CVD). The detailed process is shown in Figure 3-3. The deposition system is divided into three different chambers. The vaporization chamber holds the source material, the deposition chamber holds the substrates, and the pyrolysis chamber connects the two chambers. The deposition is performed by loading the substrates into the deposition chamber, loading the source dimer material into the evaporation chamber, pumping down to 1 mtorr, heating the

pyrolysis chamber to 670 °C, and subsequently sublimating the dimer above 150 °C. The evaporated dimer goes through the pyrolysis chamber where it is broken into monomers. The activated monomers polymerize on cool surfaces inside the deposition chamber. Parylene forms smooth conformal and pinhole-free layers that can be thinner than 100 nm. Parylene films are chemically inert, flexible, and have high electrical resistivity and low gas permeability compared to other polymers, which makes them excellent gate dielectric and encapsulation layers. Encapsulation using parylene has been demonstrated to increase storage lifetime of pentacene OTFTs [6]. Parylene is found to have sufficient adhesion to glass to have no delamination issues during cleanroom procedures such as spin-rinse dryers (SRD), dump rinsers, photoresist developers and solvent strippers.

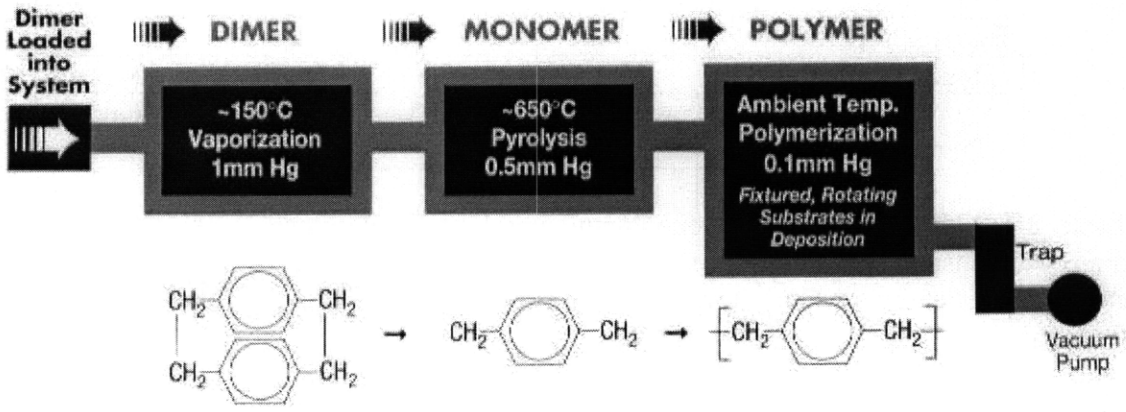

Figure 3-3: Illustration of the process flow for deposition of Parylene N. From [7].

There are several types of parylenes: the simplest one is parylene N, a polymer of benzene rings with CH_2 groups on opposite ends. Parylene C has a chlorine atom substitute for one of the hydrogen atoms in the benzene rings. Although parylene C has higher permittivity and provides better encapsulation as it is a better oxygen and moisture barrier, parylene N is used for transistors in this work because it provides permittivity that is independent of frequency.

When measuring the BSE, permittivity change caused by slow moving ionic species such as chlorine atoms in parylene C convolutes the BSE measurement. The complication in the measurement is obviated by using parylene N which has no ionic species.

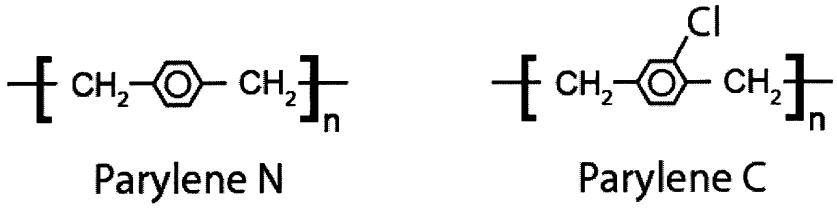

Figure 3-4: Chemical formula of parylene N and parylene C.

	Parylene N	Parylene C	
Dielectric Strength	7000	5600	V/mil
Volume Resistivity	$1.4x10^{17}$	$8.8x10^{16}$	Ωcm
Dielectric Constant			
60 Hz	2.65	3.15	
1 KHz	2.65	3.10	
1 MHz	2.65	2.95	
Barrier Properties			
O_2 gas Permeability	15.4	2.8	(cc mm)/(m^2day atm)
Water Vapor Transmission Rate	0.59	0.08	(g mm)/(m^2day)

Table 3-1: Comparison of parylene N and parylene C. Parylene N exhibits no change in dielectric constant with respect to frequency. The changing dielectric constant in parylene C causes complications when interpreting the BSE in OTFTs with parylene C dielectric. Data from [6].

150 nm-thick layer of parylene N is deposited for the gate dielectric using a Specialty Coating Systems Model PDS 2010 Labcoater 2. Via holes are patterned through the parylene dielectric by photolithography and reactive ion etching (RIE) in oxygen plasma in the Plasmaquest machine. The oxygen plasma etches both the photoresist and the parylene layer, but the thickness of the parylene layer is only 150 nm and much thinner than that of the

photoresist layer which is typically 1 μm. The thickness difference provides ample buffer to completely etch the parylene layer while leaving photoresist layer intact.

3.1.3 Source-drain and the Semiconductor

After the vias are patterned, 40 nm of gold which serves as the source-drain (S/D) layer is then deposited by e-beam evaporation. Photolithography and wet chemical etching are used to pattern the layer. Gold adheres well to parylene without an additional adhesion layer and provides good contact to pentacene. Gold is used for S/D electrodes because it has a high work function which matches the pentacene work function and provides good hole injection into the pentacene.

For the semiconductor layer, 10 – 20 nm-thick pentacene film (Luminescence Technology) is blanket deposited by thermal evaporation at a rate of 0.6 – 1.2 nm/min. The pentacene deposition system uses a Radak I evaporation system to hold the source crucible at 200 ^{o}C. The substrate is at room temperature during evaporation.

The pentacene is then encapsulated in a 200 nm-thick film of parylene, allowing the pentacene/parylene stack to be photolithographically processed without exposing the pentacene to photolithography solvents. Exposure of pentacene to the solvents has been reported to cause structural change in the pentacene film which results in discontinuous film [1]. A subsequent RIE process isolates the active area of each OTFT which is necessary to reduce leakage current from source to drain through the un-gated pentacene. Figure 3-5 shows a photo of the completed transistor and the measured output and transfer

characteristics of a 1000/5 μm device. The devices are stored in nitrogen ambient, and no measurable change in the I-V characteristics is observed over a month of storage.

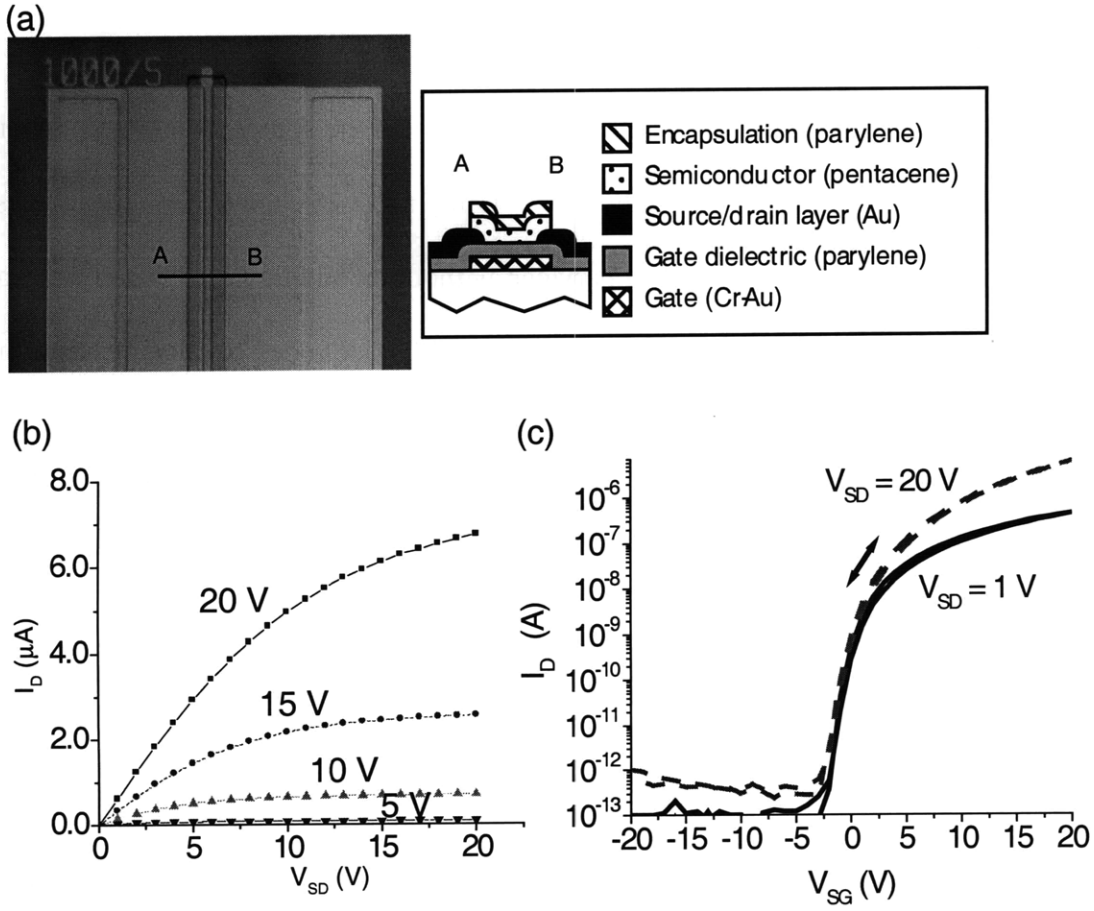

Figure 3-5: (a) Photo and the cross-section schematic of the device. (b) Output characteristics and (c) transfer characteristics of a 1000/5 μm device.

3.2 **Improvements**

3.2.1 Removal of Photoresist Residue

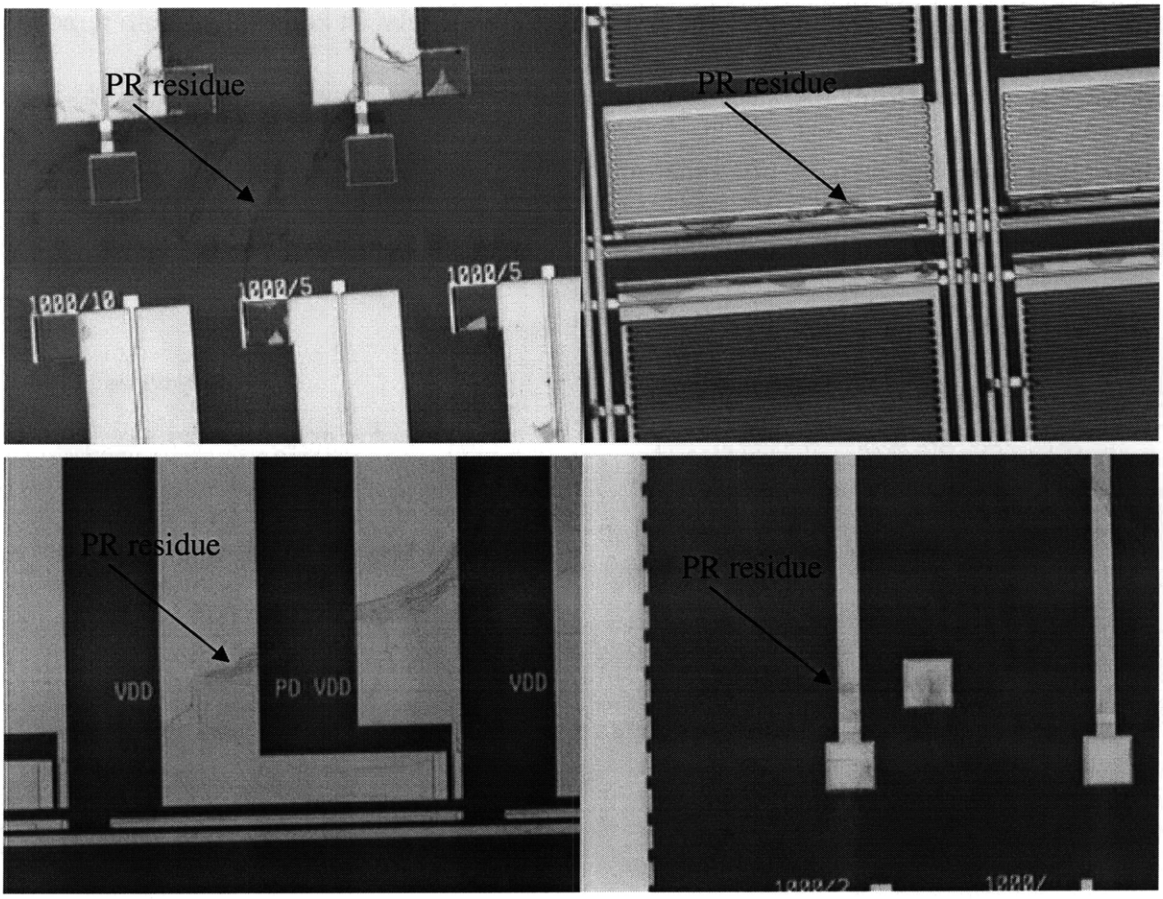

Figure 3-6: Photos of photoresist (PR) residue. The top two photos show photoresist residue after the transistors are completely patterned. The bottom two photos show that the photoresist residue is present right after the via patterning step.

After the via patterning step, a careful observation under the microscope reveals that photoresist residue is left after the RIE in oxygen plasma and the subsequent photoresist strip step as shown in Figure 3-6. The residue is due to the oxygen plasma polymerizing and hardening the photoresist, making it insoluble in Microstrip resulting in stringers. The photoresist residues are found anchored to the substrate at the via openings, where the polymerized PR layer is connected to the parylene layer as illustrated in Figure 3-7. Because

the plasma in the RIE is directional, using an image reversal resist (AZ 5214) which has negative slope leaves no hardened photoresist that is connected to the underlying parylene layer. The subsequent removal of the photoresist in Microstrip undercuts the photoresist through the unpolymerized region and removes it completely. In addition, to help remove the photoresist residue from the surface of the wafer, wafers are gently sonicated during the photoresist stripping step. A combination of these two techniques efficiently removes all photoresist residue from the via etch step.

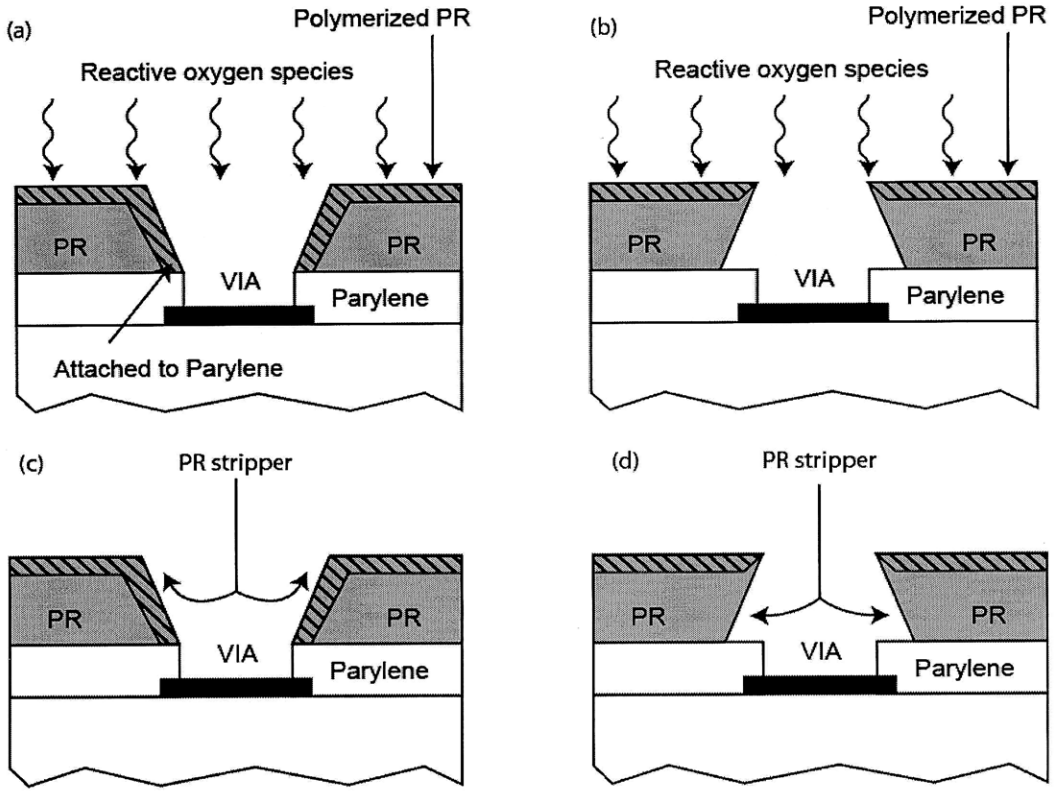

Figure 3-7: Illustration of polymerization of photoresist (PR) during RIE oxygen plasma etch. (a) The PR with positive slope will have a region where the polymerized PR is attached to the parylene. (b) In contrast, PR with negative slope does not have any region where the polymerized PR is in contact with the parylene because of the directional nature of the RIE plasma. (c,d) During photoresist removal step, the PR stripper cannot solvate the hardened PR. (d) For the PR with negative slope, the PR stripper undercuts the PR and removes it completely.

3.2.2 Sputter vs. e-beam Deposition of S/D Layer

The original process used RF plasma sputter deposition of gold on top of the parylene for source-drain layers (step 4 in Figure 3-2). However, it has been found that the oxygen plasma induces defect sites on parylene surface that acts as dopants [8]. Similarly, the argon plasma during the sputtering deposition process is also found to induce defects on the parylene surface leading to a large hysteresis as shown in Figure 3-8. Using e-beam evaporation instead of the sputtering method to deposit S/D gold layer decreases defect sites in the parylene which results in reduced hysteresis and higher current as well as sharper subthreshold slopes as shown in Figure 3-8.

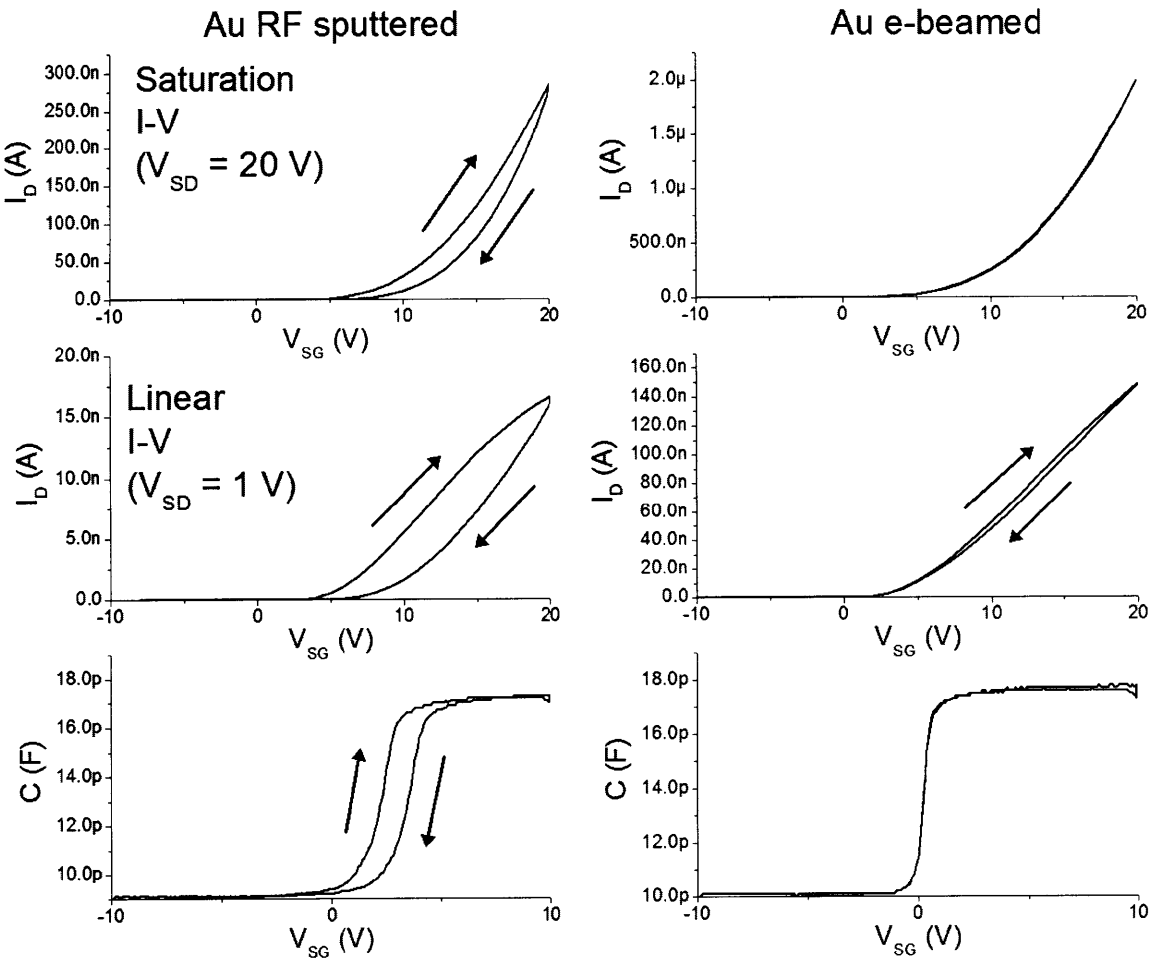

Figure 3-8: Hysteresis in OTFTs sputtered with vs. e-beamed gold S/D layer. The data in the right column are data from e-beamed S/D layer and show significantly less hysteresis as well has higher current levels. W/L = 1000/25 μm.

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Chapter 4

Characterization of OTFTs

OTFTs are field effect transistors and operate similar to Si MOSFETs. The gate, which is isolated from the semiconductor by an insulator, controls the conductivity of the semiconductor by moving its Fermi level. Typically, OTFTs are p-type semiconductors and operate in accumulation. To induce hole carriers in the channel, negative gate voltage is applied while the source is grounded as shown in Figure 4-1. The source injects holes into the channel and the drain extracts them from the channel. The structure is symmetrical between the source and the drain, and the voltage applied on the electrodes determines which one is the source. The source injects holes into the channel and is always the electrode with the higher voltage. The direction of current flow is from the source to the drain and therefore I_{SD} is positive. I_D is the current flowing out of the drain terminal and is typically the same as I_{SD} as the gate leakage current is orders of magnitude less than I_{SD}. Current should be measured from all the terminals to ensure that there are no other leakage paths.

Unlike MOSFETs, OTFTs operate in accumulation rather than in inversion because it is easier to accumulate charge in the channel. Accumulation mode of operation is possible

because the semiconductor is not connected to a body electrode, which would leak out majority carries. Also it is difficult to achieve electron carrier transport in pentacene because electron mobility is low, and it is difficult to move the Fermi level across the bandgap. In addition, injection of electrons from the high work function electrodes is difficult.

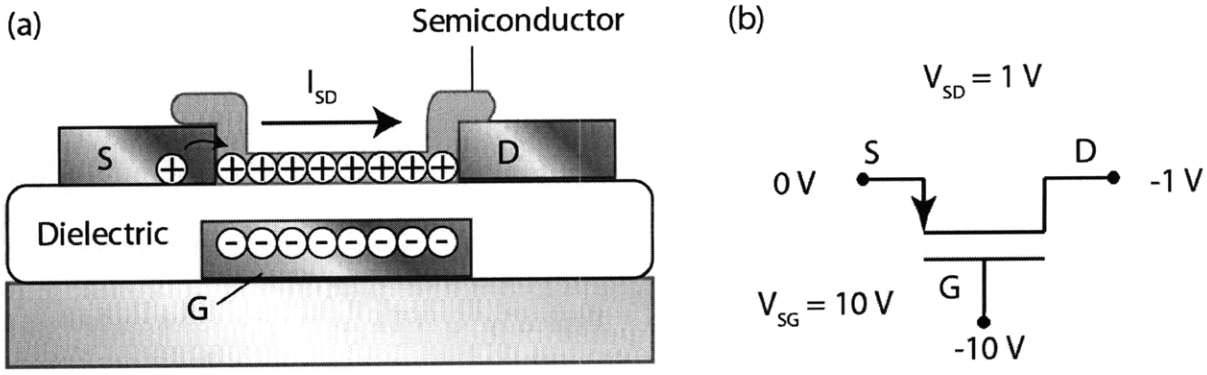

Figure 4-1: Operation and symbol of a pentacene OTFT

4.1 Measurements

I-V characteristics are taken using the Agilent 4156C parameter analyzer. The 4156C has the capability to measure currents as low as 1 fA and to take transient and capacitance-voltage measurements. It has four source measurement units (SMUs) which are able to supply voltage or current and measure the other.

When measuring I-V characteristics of OTFTs, it should be noted that measurement parameters such as hold time, delay time, and integration time affect the measurement. Hold time is the duration that the system holds the start voltage before the first measurement.

Delay time is the time that the system holds the voltage between the measurements. Lastly integration time is the time during which the measurement is taken and averaged out. The integration time can be varied from 60 μs to 100 s, with 16 ms for medium integration time. The delay and hold times should be optimized; if the delay time is too short, the current is measured before the channel carriers have had a chance to equilibrate. In contrast, if the measurement takes too long, degradation is induced during the measurement, which results in hysteresis and lower currents as the measurement progresses.

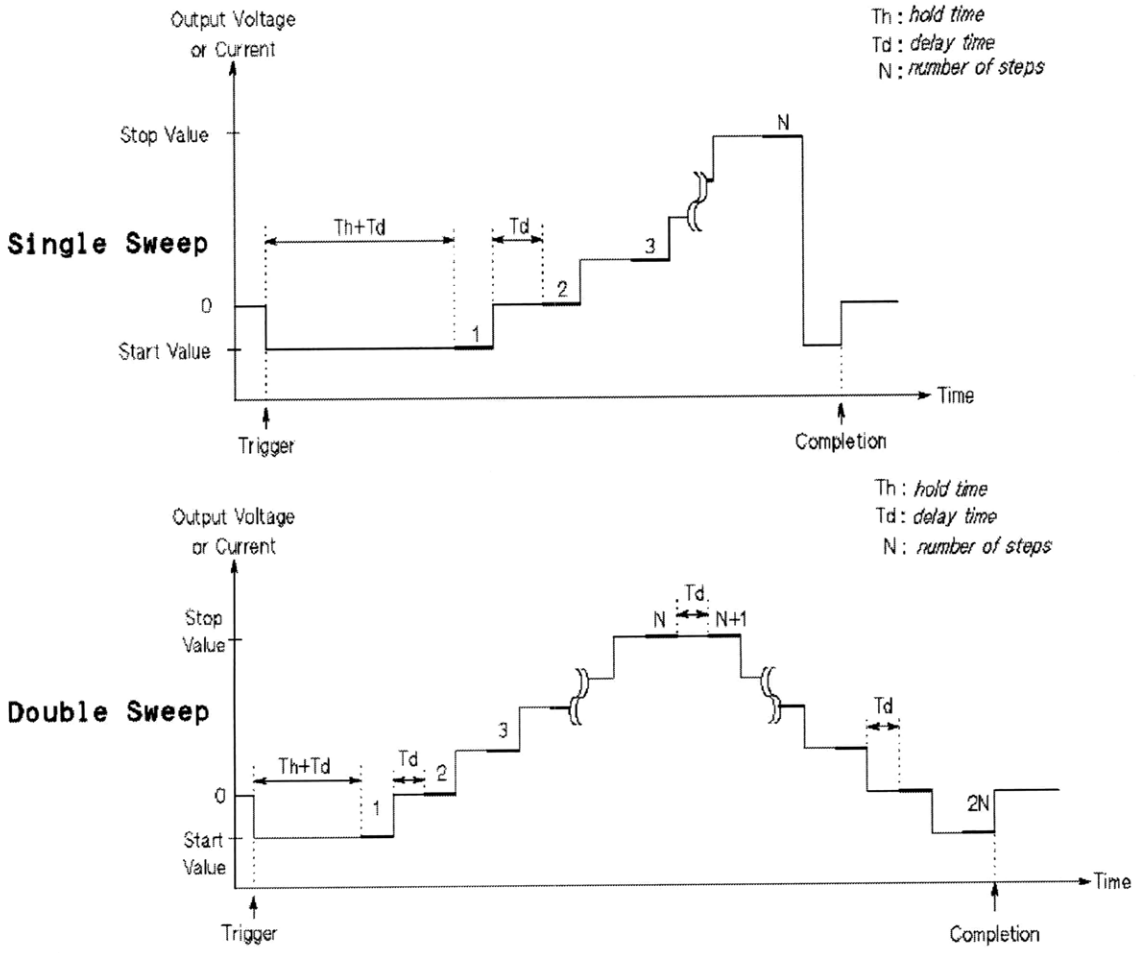

Figure 4-2: Sequence of measurements showing the definition of hold time, delay time, and integration time for single and double sweeps. From [1].

The time it takes for a transistor to reach equilibrium can be calculated from the RC time constant of the transistor. A simplified model of one capacitor, which has the value of the channel capacitance at the middle of the channel where it can be accessed by two resistors with $R_1/2$, where R_1 is the channel resistance, is shown in Figure 4-3. This transistor has a RC time constant of $R_1C_{CH}/4$. If I_D of 1 pA at V_{SD} = 0.1 V, or $R_1 = 10^{11}$ Ω, is to be measured accurately for a transistor with channel capacitance of 1 pF, $R_1C_{CH}/4$ = 25 ms, so a delay time of 100 ms should be used.

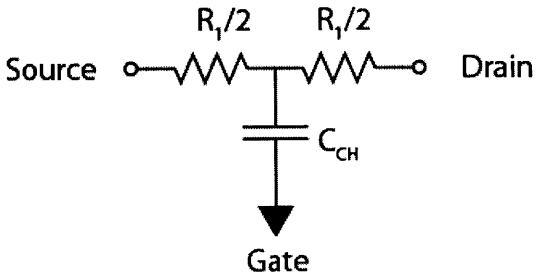

Figure 4-3: Model for calculating time constants for measuring accurate current.

The hold time affects I-V characteristics in a similar manner. If the hold time is too short, the channel is not in equilibrium. If the hold time is too long, the measurement causes degradation in the channel. To avoid causing the bias-stress effect during I-V characteristics, the gate voltage is swept from off (V_{SG} is negative) to on (V_{SG} is positive) with optimized delay and hold times of 100 ms and 1 s. Repeated I-V characteristics measurements show that the change in gate voltage caused by the measurement is less than 0.1 V for standard measurements described in Appendix B.

Capacitance-voltage (C-V) measurements are useful in understanding how much charge is in the channel. In OTFTs, quasi-static C-V (QSCV) measurements are needed because the low carrier mobility and high contact resistance increase access time of the carriers to the channel. The QSCV measurement is taken by slowly changing the gate voltage while both source and drain are tied together to ground. Change in voltage induces current in a capacitor:

$$I = C\frac{dV}{dt} \tag{4-1}$$

The leakage current is accounted for by taking leakage current measurements before and after the ramp. The 4156C integrates the charge during the small voltage step and subtracts the charge due to this leakage current to measure the capacitance:

$$\Delta Q - \Delta Q_{leak} = C\Delta V \tag{4-2}$$

where ΔQ is the total charge measured, and ΔQ_{leak} is the I_{leak} multiplied by the integration time.

Temperature and ambient atmosphere should be controlled and monitored during measurements as temperature is known to increase current, and humidity has been reported to affect the transistor characteristics [2].

4.2 **I-V Characteristics**

The transistor is separated into two different regions of operation depending on the V_{SG}. The subthreshold region is when $V_{SG} < V_T$. The drain current rises exponentially as the gate voltage approaches the threshold voltage. This region is marked by relatively small number of states in the forbidden region between highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) which does not hinder the movement of the Fermi level. The threshold voltage is empirically defined from a semilog plot of the transfer characteristics. It is defined as the point where the drain current deviates from a straight line in the subthreshold region as shown in Figure 4-4. Traditionally threshold voltage refers to the gate voltage where the transistor is at the threshold of inversion, as MOSFETs turn on when the channel is inverted. The voltage at which OTFTs turn on should be termed the flatband voltage because OTFTs operate in accumulation. Nonetheless, we use the term threshold voltage to be consistent with the Si MOSFET literature.

In the subthreshold region, the drain voltage has little effect on the drain current above 1 V. It can be approximated by the following equation derived for MOSFETs [3]:

$$I_D = I_{off} \exp(V_{SG}/nV_{th})(1-\exp(-V_{SD}/nV_{th}) \qquad (4\text{-}3)$$

where I_{off} is the current when $V_{SG} = 0$ V at a sufficiently high V_{SD} ($> 3nV_{th}$), and n is the non-ideality factor which is extracted from the subthreshold slope, and V_{th} is the thermal voltage which is about 26 mV (=1/kT) at room temperature. The subthreshold slope (S) is also extracted from the semi-log plot of transfer characteristics as shown in Figure 4-4.

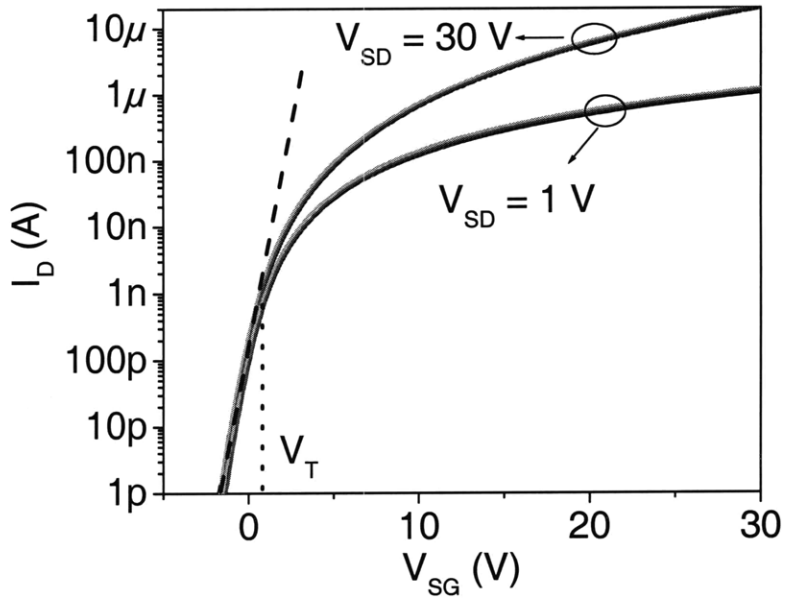

Figure 4-4: Transfer characteristics of six different devices in linear (V_{SD} = 1 V) and saturation (V_{SD} = 30 V) region. The V_T is the V_{SG} that the current deviates from a line in the semilog plot. The inverse slope of the line is the S [V/dec].

In the above threshold region $V_{SG} > V_T$, the Fermi level is close to the HOMO, and its movement is hindered greatly by the existence of many shallow trap states. This results in much slower increase in the current. When $V_{SD} < V_{SG} - V_T$, the current increases linearly with V_{SD}, and this region is called the linear region. The drain current can be described similar to MOSFETs:

$$I_D = W/L\, C_i\, \mu\, (V_{SG} - V_T - \tfrac{1}{2}V_{SD})\, V_{SD} \qquad (4\text{-}4)$$

where W, L is the width and length of the OTFT [μm], C_i is the channel capacitance [F/cm^2].

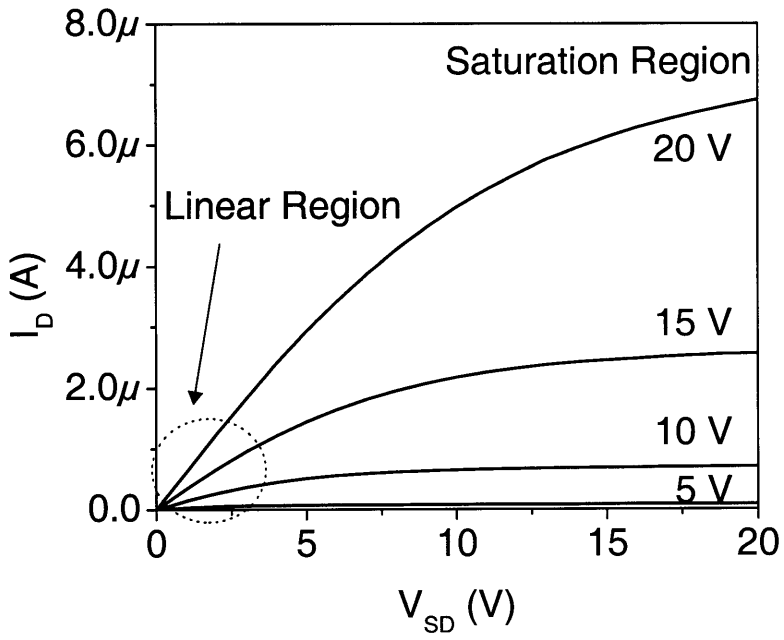

Figure 4-5: Output characteristics of an OTFT. The left region where $V_{SD} < V_{SG} - V_T$ is the linear region.

One notable difference from MOSFETs is that in OTFTs μ increases with gate voltage leading to I_D dependence that is super-linear on V_{SG}. In addition, the existence of contact resistance complicates this simple picture. The effects of contact resistance must be taken into account for accurate mobility measurements.

4.3 **Contact Resistance**

Contact resistance can be significant in OTFTs and must be extracted. The origin of the high contact resistance can be either the Mott-Schottky (MS) barrier due to the Fermi level mismatch of the semiconductor and the metal or the highly resistive area near the source-drain electrodes in the case of bottom-contacts. Because Au work function (5.4 eV) is closely

matched to the HOMO level of pentacene (5.2 eV), little MS barrier is expected. However, it is found that dipoles build up near the Au/pentacene interface which can shift the vacuum level as much as 1 eV and create MS barriers [4]. The dipole is formed as the tail states in the pentacene near the HOMO are filled with holes. The highly resistive area near the source-drain electrodes are formed by different surface energy of parylene and Au. This difference causes pentacene growth to be different on the two surfaces, and at the boundaries of the two different growths, the pentacene grains are strained, leading to regions with smaller grain sizes, and lower mobility [5]. If the contact resistance is mainly caused by the MS barrier, the drop at the source electrode will be the dominant source of contact resistance. However, it has been reported that for some contacts, the drop is equally distributed at the source and drain electrodes. This behavior has been attributed to the highly resistive pentacene region near the electrodes.

The contact resistance can be measured in a number of methods: Kelvin probe measurements, four-point probe measurements and transmission line method (TLM) [6]. Unlike the other two methods, the TLM requires neither a special apparatus nor a special structure. The TLM measures contact resistance by measuring resistance of different length transistors. The resistance measured at a given gate voltage is plotted vs. the channel length as shown in Figure 4-6. The resistance measurement is calculated from the transfer characteristics taken in the deep triode region with V_{SD} = 1 V. In the deep triode region where $V_{SD} << V_{SG} + V_T$, Equation (4-4) can be simplified to yield the following expression for the channel resistance:

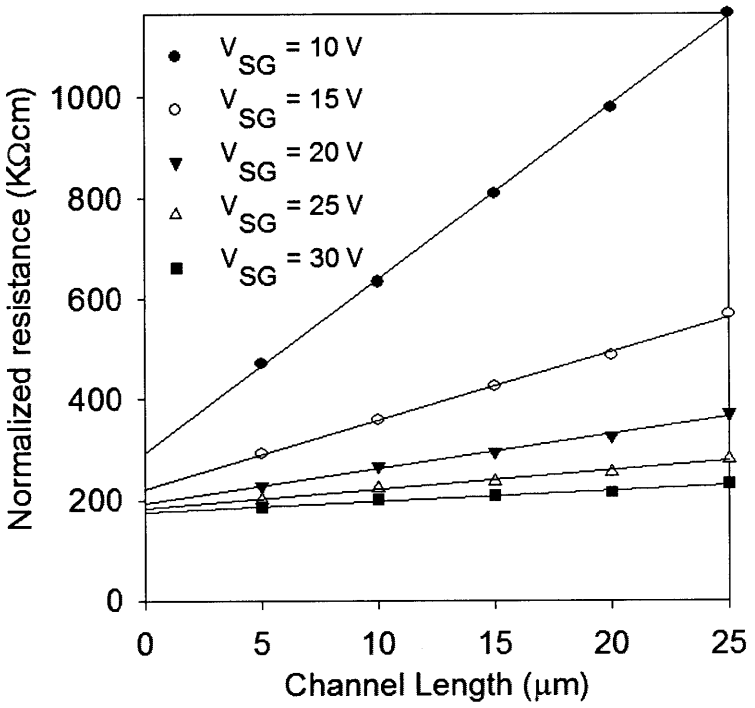

Figure 4-6: Extraction of contact resistance using the TLM. The resistance extrapolated at L = 0 is the contact resistance. The data is denoted by symbols, and solid lines are fits made for each gate voltages.

$$V_{SD}/I_D = L/WC_i \mu (V_{SG} - V_T) \qquad (4\text{-}5)$$

The measured resistance in the transistor is the sum of this channel resistance and the contact resistance:

$$R = \frac{L}{WC_i \mu (V_{SG} - V_T)} + R_C \qquad (4\text{-}6)$$

where R is the measured resistance, and R_C is the contact resistance. Both sides of the equation are multiplied by W to normalize the measured resistance with respect to width for comparison with measurements from different width transistors. From the relationship, the

contact resistance can be easily extracted from a linearly extrapolated resistance at L = 0. For the TLM to work, the contact resistance must be uniform in all the measured transistors. This can be justified by the good linear fit on the measured resistance data as shown in Figure 4-6. The extracted contact resistance is highly non-linear and gate voltage dependent as it has been reported for other OTFTs measured using other methods [7,8,9,10] as well as the TLM [11,12,13].

Once the contact resistance is known, the mobility can be extracted from an I-V measurement in the linear region and a QSCV measurement [14]. In the deep triode region, the channel carrier distribution is uniform from source to drain. Therefore the velocity of the carriers and the electric field across the channel are uniform. The uniform electric field allows us to find the electric field by simply dividing the voltage dropped across the channel by the channel length. The following equations for a straightforward extraction of mobility result from the uniform electric field:

$$I_D = W\,Q\,E\mu$$
$$E = (V_{SD} - I_{SD}\,R_c)/L \qquad (4\text{-}7)$$

Since Q can be measured from the QSCV measurement, and all other variables are known or measured, mobility can be extracted from the combination of I-V and QSCV measurements. When extracting mobility, accounting for the contact resistance is important as illustrated in Figure 4-7. Not accounting for the contact resistance can result in a deceiving dependency of mobility on the channel length. The OTFTs with shorter channel lengths have smaller

mobility as it is affected more severely by the contact resistance. In addition, the presence of high contact resistance can mislead one to think that mobility is independent of gate voltage as shown for 5 μm device between V_{SG} = 15 V and 20 V. Many claims of gate voltage independent mobility in OTFTs are due to not accounting for the contact resistance [15]. After correcting for the contact resistance, mobility is independent of channel length and increases with V_{SG}.

Every time a wafer is made, various parameters including contact resistance and mobility are extracted with standardized I-V and C-V measurements to monitor the process, and make sure that the process stays within the expected process variations. The methods of extraction and definition of various parameters are listed in Appendix B. Typical parameters extracted from transistors are also available there.

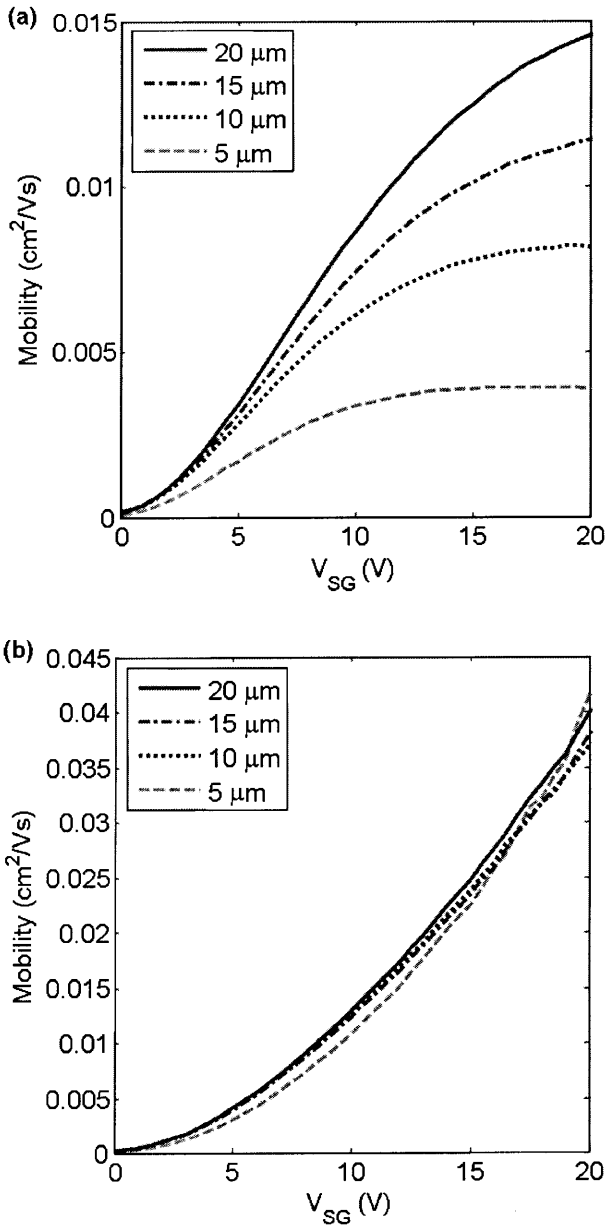

Figure 4-7: Extracted mobility according to a simplified physical model in Equation (4-7). (a) Not accounting for the contact resistance. (b) Accounting for the contact resistance. If the contact resistance is not accounted for, the mobility decreases severely on shorter channel-length devices. This is because devices with shorter channel lengths are affected more by the contact resistance. In addition the mobility for 5 μm device looks as if it is constant with respect to the gate voltage. This is not true once the mobility is corrected for the contact resistance.

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Chapter 5

The Bias-stress Effect in Pentacene Organic Thin-film Transistors

5.1 Introduction to the Bias-stress Effect

Instabilities in OTFTs have been reported for a wide range of semiconductors and structures. The initial studies of instability in OTFTs focused on degradation due to exposure to oxygen and moisture. Exposure of organic semiconductors to these reactive species has been known to degrade the performance in OLEDs [1,2]. It has been found that exposure of OTFTs to ambient air leads to instabilities resulting in degradation of mobility and a shift in threshold voltage [3].

Identification of degradation due to reactive species has led to the development of encapsulations and more stable organic semiconductors. With the developments in these fields, the exposure of OTFTs to ambient air no longer degrades the device performance significantly. Someya *et al.* have reported devices with organic/metallic hybrid encapsulation that show stable characteristics even after two months of ambient air exposure [4].

Demonstration of stable transistors under ambient storage has led to a shift in the focus of research to instabilities caused during operation of the transistors. OTFTs exhibit the bias-stress effect (BSE) – the change in I-V characteristics due to prolonged bias voltages. The BSE causes operational instability in OTFTs that leads to reliability shortcomings that must be addressed for practical circuit applications of these transistors.

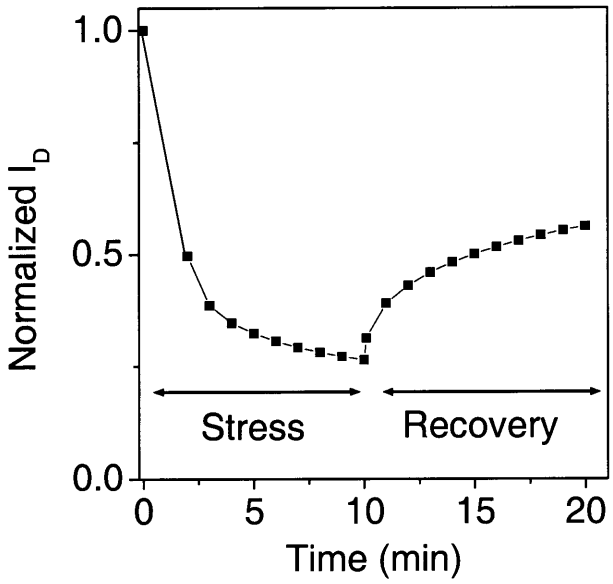

Figure 5-1: Change in the drain current due to the BSE. The plot shows normalized drain current measured at V_{SG} = 10 V, V_{SD} = 1 V during stress phase (V_{SG} = 30 V applied between measurements), and recovery phase (V_{SG} = 0 V) in nitrogen ambient. When stress is applied, the current degrades. Upon removal of the stress, the current recovers.

Figure 5-1 shows the drain current change due to the BSE. When the bias is applied the BSE reduces the current that flows through the transistor. Upon removal of the bias, the current starts to recover. Given enough time, transistors are found to recover the original I-V characteristics as shown in Figure 5-2. Such recovery of the degradation due to the BSE in OTFTs has also been reported elsewhere [5].

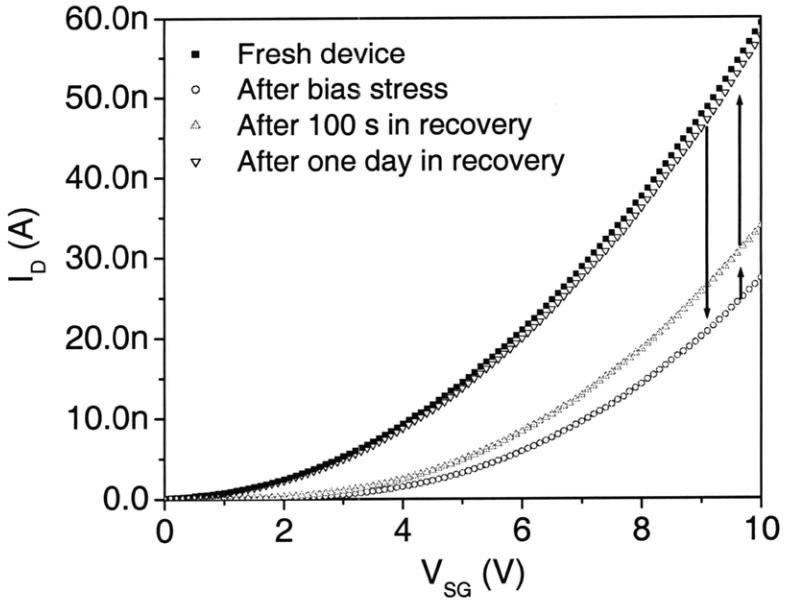

Figure 5-2: I-V transfer characteristics before, after stress, after 100 s of recovery, and after a day of recovery. The stress condition was V_{SG} = 30 V for 100 seconds. Recovery is performed by grounding the terminals in the dark. Transfer characteristics were taken at V_{SD} = 1 V. Measurements were taken on a W/L = 1000/25 μm device in nitrogen ambient in the dark.

The mechanisms of the BSE in OTFTs are mostly unknown. Moreover, few systematic and quantitative studies of the BSE have been completed to date. Many studies have been limited to observations of hysteresis in the I-V characteristics of TFTs [6,7], or have primarily focused on reducing the BSE with the use of different semiconductors and device processes. Selected studies on pentacene OTFTs are summarized here. Brown *et al.* have reported that when transistors with pentacene or poly(thienylene vinylene) on SiO_2 dielectric are stressed with DC gate bias, the drain current decreases [8]. They report that the degradation is reversible at room temperature and can be accelerated by applying a reverse bias. Many reported that moisture has a significant effect in accelerating the BSE. For example, Komoda *et al.* have measured pentacene transistors with SiO_2 dielectric in different ambient conditions such as vacuum, dry air, and ambient air and conclude that moisture causes

additional degradation on top of the degradation that occurs in vacuum or dry air [9]. They propose movement of ionic species (H^+ or OH^-) to be the cause of the accelerated degradation. Effects of moisture can also be inferred from Kagan *et al.*, which reports amount of degradation is significantly reduced when devices are tested in nitrogen compared to ambient air [10].

Most existing studies on the BSE in OTFTs are lacking for one or more of the following three reasons. First, published works have been predominantly conducted on thermally grown SiO_2 gate dielectric with unpatterned gates. For flexible large-area electronic applications, thermally grown SiO_2 cannot be used due to thermal budget, and the gates must be patterned. Moreover, it has been reported that for devices with SiO_2 gate dielectric, the measured BSE may be due to water-related charge trapping at the SiO_2 surface rather than due to trapping in the organic semiconductor itself [11]. The paper uses the finding to explain why similar BSE behaviors have been found in TFTs with many different organic semiconductors. Therefore, to study the relevant BSE which can be applied to devices that can be used in flexible large-area applications, devices with gate dielectrics compatible with flexible substrates must be used.

Secondly, most studies measure the BSE in ambient air and use transistors with no encapsulation. It has been established that storage in oxygen and moisture ambient degrades the semiconductor. In order to study the characteristics of the BSE, these extraneous effects should be avoided by measuring in nitrogen ambient or using adequate encapsulation. Ute *et al.* have tried to separate out the degradation due to storage in air and degradation due to the

BSE by comparing the performance of a transistor that has been stored in air with that of a transistor that has been stressed [12]. Although it may be possible to make valid inferences of the BSE through this method, it is better to study the BSE in transistors with proper encapsulation, in nitrogen ambient to ensure that only the degradation due to the BSE is measured.

Thirdly, most works do not conduct a systematic study of the BSE at different bias-stress conditions. Sekitani *et al.* have overcome the two shortcomings listed above by measuring the BSE in integrated OTFTs with encapsulation and a polymeric gate dielectric in nitrogen ambient [13]. However they have primarily focused on demonstrating that the annealing process can be used to improve device stability, and the BSE has been only investigated at a single bias-stress condition of fixed V_{SD} and V_{SG}. In order to understand the BSE and model it for circuit lifetime estimations, the BSE at different stress conditions must be measured. This work addresses these shortcomings by systematically studying the BSE on integrated OTFTs with patterned gates and parylene polymer dielectric. The completed devices have sub-picoamp gate leakage current and exhibit no measurable change in I-V characteristics over a month of storage in a nitrogen box.

Although the BSE has been reported in a-Si:H TFTs as well, there are notable differences. In a-Si:H TFTs, the BSE is not reversible at room temperature. During fabrication, a-Si:H TFTs are annealed at higher temperatures in hydrogen ambient to deactivate dangling bonds either by forming weak Si-Si bonds or hydrogenating them. At room temperature, the a-Si:H is not in equilibrium, and dangling bonds are created when hydrogen atoms are released from Si-H

bonds and break weak Si-Si bonds when electrons are present [14]. This chain reaction illustrated in Figure 5-3 results in two dangling bonds, which become electrically active sites for trapping electrons. This process of trap creation explains light-induced defect creation in a-Si:H TFTs [15]. The same process accounts for the BSE in a-Si:H TFTs. Upon flooding the channel with carriers, the weak Si-Si bonds break and become dangling bonds which act as trap sites [16, 17]. The a-Si:H TFTs must be annealed at higher temperature to recover the original I-V characteristics [18].

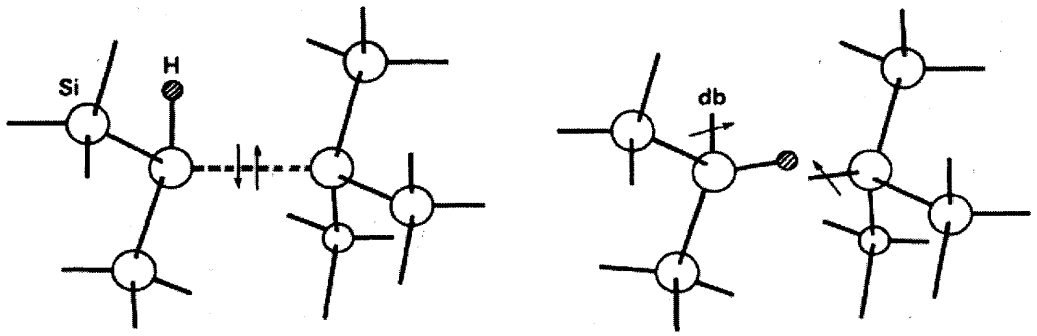

Figure 5-3: Defect creation mechanism in a-Si:H. Weak Si-Si bonds are broken upon occupation of two electrons and stabilized with movement of the hydrogen from a nearby site. The process causes two new dangling bonds which act as electron trap sites. From [15].

The origin of the BSE in pentacene OTFTs is different as pentacene has no silicon bonds that could break to form trap states. It has robust C=C bonds which have higher bond strengths (6.3 eV) than Si-Si bonds (2.3 eV) and are in equilibrium at room temperature evidenced from the full recovery of the BSE at room temperature and no report of light-induced defect creation in pentacene OTFTs. As expected, the BSE in a-Si:H TFTs continue until there are no more carriers in the channel because of the abundance of weak Si-Si bonds [16,19]. However in pentacene OTFTs, we find that BSE saturates even in the presence of free

carriers in the channel. The different origin of the BSE and the high bond strengths of C=C bonds in pentacene OTFTs may ultimately lead to TFTs with less BSE and better operational stability, which can be used in a wide range of large-area electronics.

5.2 I-V Stress Characterization

To first analyze the effects of the BSE on the overall I-V characteristics, transfer and output characteristics, are measured on a fresh device. To avoid other degradation mechanisms, measurements are carried out in nitrogen ambient with 0 % relative humidity (RH). Measurements are taken using an Agilent 4156C semiconductor parameter analyzer on a Signatone S-250 wafer prober with a Silicon Thermal PowerCool temperature controlled chuck. All stress measurements are taken in the dark and at 20 ^{o}C unless noted otherwise.

After application of bias stress, the I-V characteristics shifts to the right in the V_{SG} axis as shown in Figure 5-4. The shape of the new I-V characteristics is nominally identical to the one before stress. This is illustrated by the overlay of the shifted original I-V characteristics with the one after stress. For the example stress of V_{SG} = 30 V and V_{SD} = 1 V applied for 100 seconds, the gate voltage shift is the same in both linear and saturation regions as depicted in Figure 5-4. The gate voltage shift, ΔV, can be used to characterize the BSE in both linear and saturation regions.

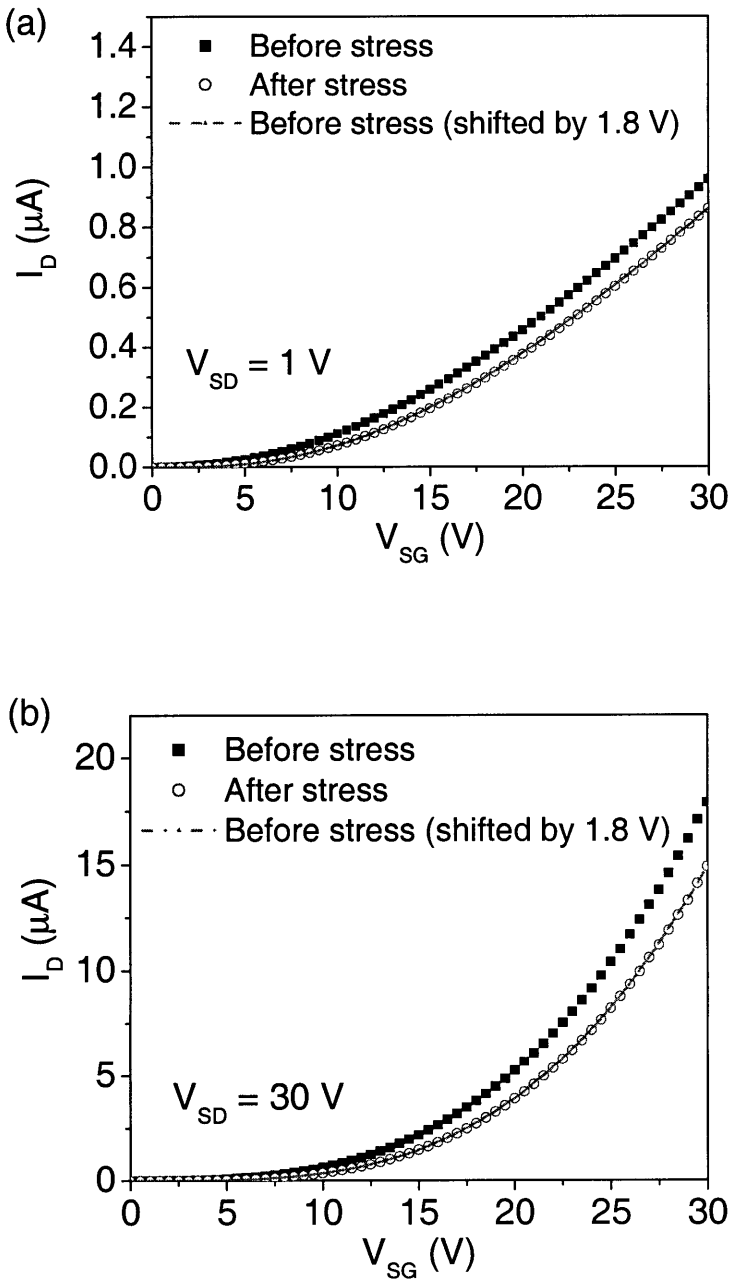

Figure 5-4: (a) Transfer characteristics in the linear region before and after stress. (b) Transfer characteristics in the saturation region before and after stress. The dotted green line shows the original I-V characteristics shifted by 1.8 V to the right for visual aid for comparisons. The data indicates that I-V characteristics after stress can be characterized by a shift in the gate voltage for both linear and saturation regions. The stress condition was V_{SG} = 30 V, V_{SD} = 1 V for 100 s.

The measurement sequence of I-V, stress, and subsequent I-V can be done to measure the ΔV caused by the BSE. This measurement is termed the I-V stress characterization method. The sequence of measurements is automated in *LabVIEW* to minimize error that can be introduced by instrument-setting time between the measurements. Figure 5-5 shows the resulting transfer characteristics measurements for a stress V_{SG} of 30 V and V_{SD} of 1 V for increasing stress time. We observe that the applied stress shifts the transfer characteristics in the positive V_{SG} direction. This shift results in reduced current for a fixed bias.

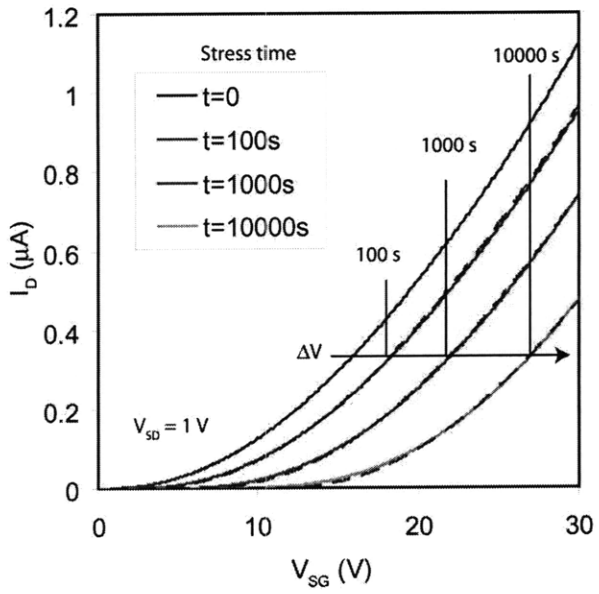

Figure 5-5: Transfer characteristics as a function of the stress time. The I-V transfer characteristics are taken by interrupting the bias stress. The stress condition is V_{SG} = 30 V, V_{SD} = 1 V. The dashed lines show the shifted transfer characteristics of the fresh device for visual aid.

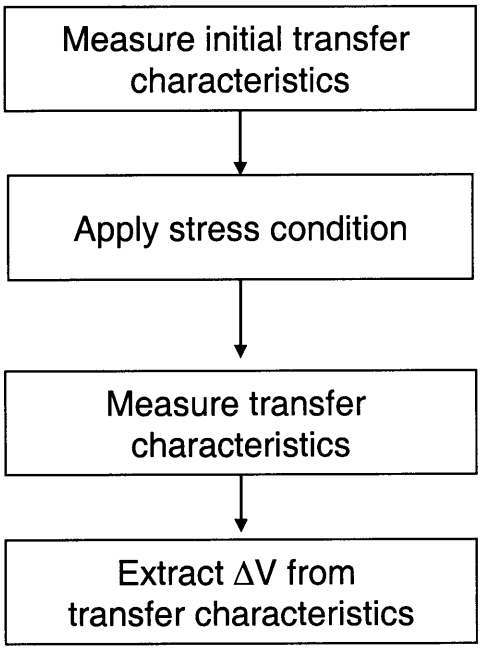

Figure 5-6: Flow chart for the I-V stress characterization method.

5.2.1 Channel Length Dependence

Channel length dependence of the BSE is studied by measuring ΔV after identical stress conditions of V_{SG} = 30 V, V_{SD} = 0.1 V at room temperature for five minutes on devices with 5, 10, 15, 20, 25 μm channel lengths. After application of stress for five minutes, the devices are then grounded and measured every minute to measure the recovery from the BSE. Length dependence provides insight into the mechanisms of the BSE and its recovery. Because the BSE can be characterized by ΔV, it can be modeled by trapping of the channel carriers, where ΔV is proportional to the amount of trapped carriers. This trapping process can be modeled as a two part mechanism where the carriers first transport from the source contact to the vicinity of the traps, and then the carriers are trapped as illustrated in Figure 5-7. The recovery, vice versa, can be modeled by carriers first detrapping from the traps and then transporting out of the channel. The transport time during the stress is expected to be

negligible because the channel is conductive at V_{SG} = 30 V. However, during the recovery when V_{SG} = 0 V, the channel is highly resistive, and the time to transport the detrapped carriers out of the channel can be long. It may even be possible that the detrapped carriers are trapped again while they are transported out of the channel.

The measured data shown in Figure 5-8 indicates that there is no length dependence during both stress and recovery. The data indicate that the rate limiting step in the BSE and its recovery is the trapping and detrapping of the carriers at the trap sites. In addition, they indicate that the transistors of different channel lengths have identical BSE.

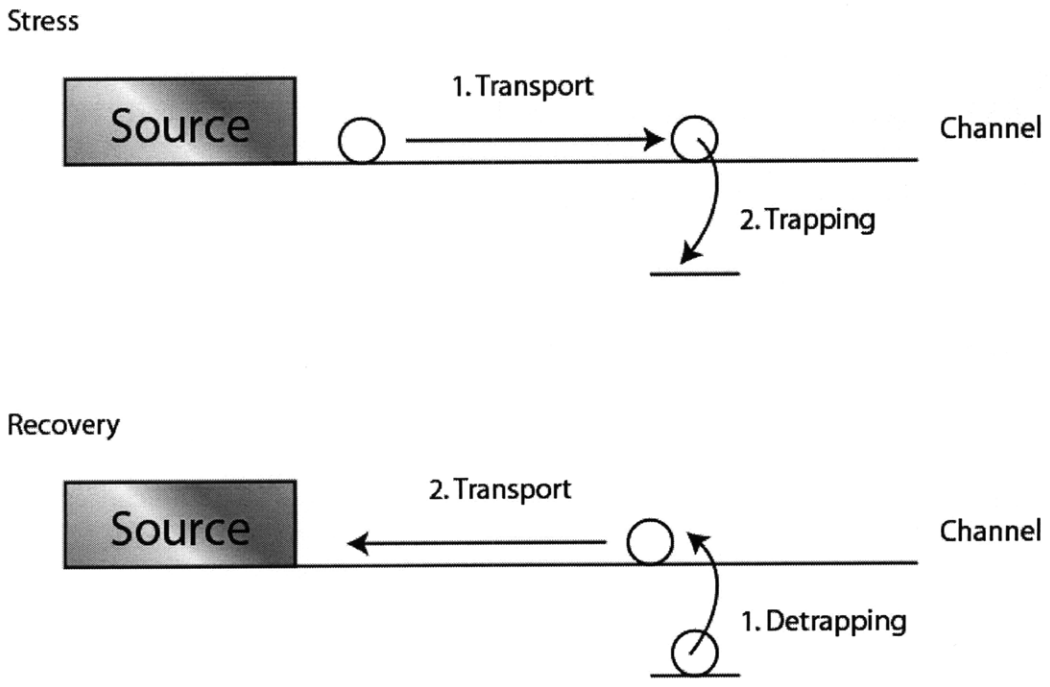

Figure 5-7: Mechanisms for the BSE and its recovery. The mechanism has two parts where the hole transports to the vicinity of the trap and then is trapped.

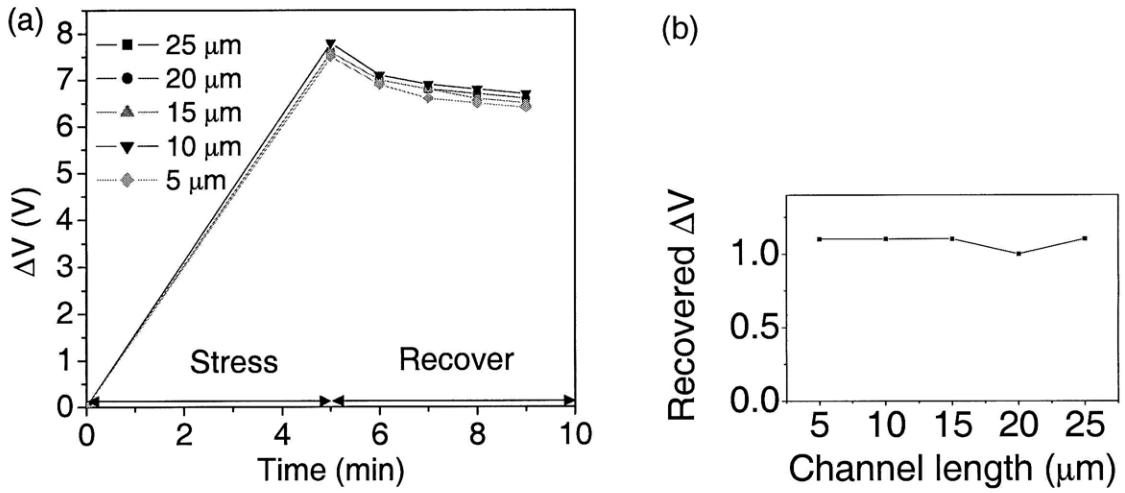

Figure 5-8: (a) Plot of ΔV after stress and recovery for different length transistors. The device is stressed for 5 minutes at V_{SG} = 30 V and then grounded for 5 minutes to recover. (b) Recovered ΔV after five minutes of recovery.

5.2.2 Voltage Dependence

The BSE is caused by the presence of both field and the channel carriers. Gate voltage dependence of ΔV supports this point. ΔV is measured after stress conditions of varying V_{SG} on fresh 1000/5 μm devices, with V_{SD} = 1 V and stress time = 100 s. Figure 5-9 shows ΔV with respect to the stress V_{SG}. When stress $V_{SG} > 0$ V the transistor is on and the channel is filled with carriers. The carriers then get trapped which leads to increase in ΔV. At similar gate voltages of opposite polarity, $V_{SG} < 0$ V, the channel is off with no carriers, and the ΔV is negligible. One more measurement supports the need for both carriers and field for the ΔV to occur. When the channel is only supplied with carriers by soaking it in light, there is no observable change in I-V characteristics as shown in Figure 5-10.

The ΔV dependence on V_{SG} can be modeled by:

$$\begin{aligned} \Delta V &= K(V_{SG})^n \quad \text{if } V_{SG} > 0 \\ \Delta V &= 0 \quad \text{if } V_{SG} < 0 \end{aligned} \tag{5-1}$$

where K is a constant, and n ~ 3.

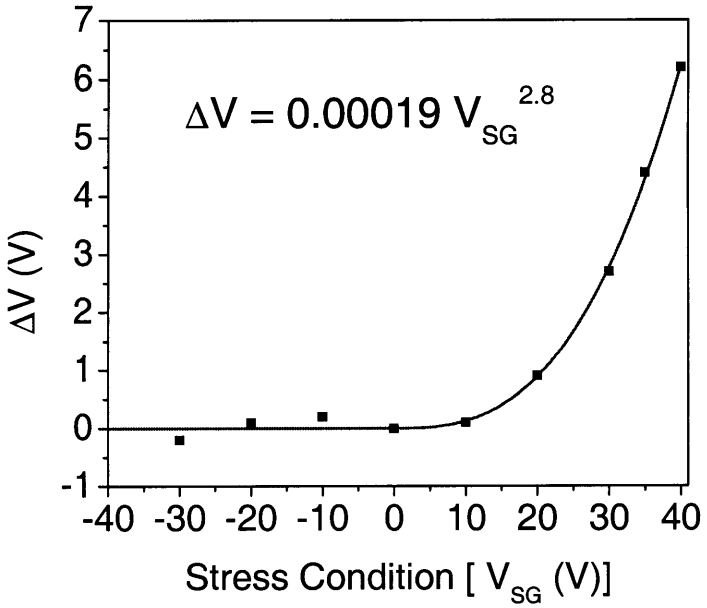

Figure 5-9: ΔV measured after different stress V_{SG} condition. Measurements are taken on fresh 1000/5 μm devices with V_{SD} = 1 V, stress time = 100 s at room temperature. The solid line is a fit made according to Equation (5-1).

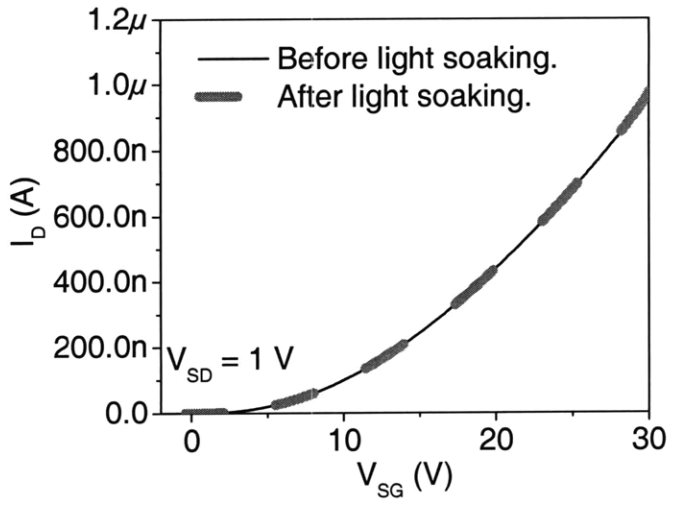

Figure 5-10: I-V measurement before and after soaking OTFT in microscope light for 10 minutes. No change in I-V characteristics is observed.

The observation that both the gate field and channel carriers are needed to induce the BSE is strengthened by studying the drain bias dependence. As the drain bias during stress increases, the resulting ΔV decreases as shown in Figure 5-11 (a). The measurement is taken by varying V_{SD} during stress while keeping other conditions equal (V_{SG} = 30 V, stress time = 600 s). It is notable that while the current increases from zero at V_{SD} = 0 V to tens of μA at V_{SD} = 30 V, the ΔV decreases indicating that current and hot carriers are not the cause of the BSE. Figure 5-11 (b) replots the data with respect to charge in the channel at different V_{SD}. The charge in the channel is calculated from the following equation [20]:

$$Q = \frac{2C_i WL}{3} \frac{(V_{SG} - V_{T0})^3 - (V_{DG} - V_{T0})^3}{(V_{SG} - V_{T0})^2 - (V_{DG} - V_{T0})^2} \qquad (5\text{-}2)$$

where C_i is the normalized capacitance of the dielectric [F/cm^2], W, L are width and length of the active layer respectively, and V_{T0} is the initial threshold voltage. As V_{SD} increases, accumulation charge density at the drain end of the channel decreases resulting in less charge in the channel. The ΔV measured for different V_{SD} scales linearly with charge in the channel indicating that when V_{SG} is the same, ΔV is proportional to the charge in the channel. Similar observations have been made by others in pentacene OTFTs on SiO_2 by Zan and Kao [21].

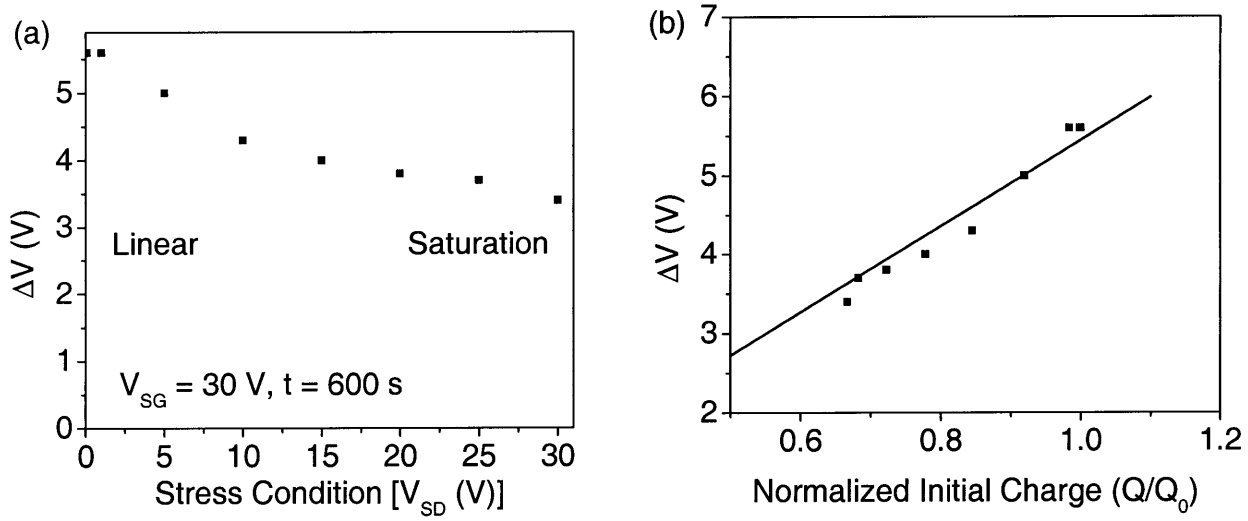

Figure 5-11: (a) ΔV vs. stress V_{SD} at t = 600 s. The V_{SG} during stress was held at 30 V. The induced ΔV decreases with increasing V_{SD}. (b) Data replotted in normalized charge. Q is calculated with equation (5-2) and $Q_0 = C_i(V_{SG} - V_{T0})$. The solid line represents a linear fit.

5.3 **On-the-fly Stress Characterization**

To study stress time dependency of the BSE using the I-V stress characterization method, I-V sweeps must be taken intermittently between stress conditions. Measuring the BSE using this method is not ideal because the intermittent I-V sweeps interrupt the stressing phase and introduce additional stress on the device. The unchanging transfer characteristics shape

allows us to measure current while the device is under stress and extract ΔV by looking up V_{SG} for the measured current on the original transfer characteristics. The flowchart of the implemented measurement is shown in Figure 5-12. This measurement is termed the on-the-fly stress characterization method. This method of characterizing stress is preferable to the I-V stress characterization method because there is no measurement error introduced by the intermittent I-V sweeps. Although some error introduced by the initial I-V sweep is unavoidable, this error is relatively small as the device is held at stress conditions for less than a second. In addition this method allows ΔV measurement at stress times as short as one second which is necessary for the study of time dependency of the BSE.

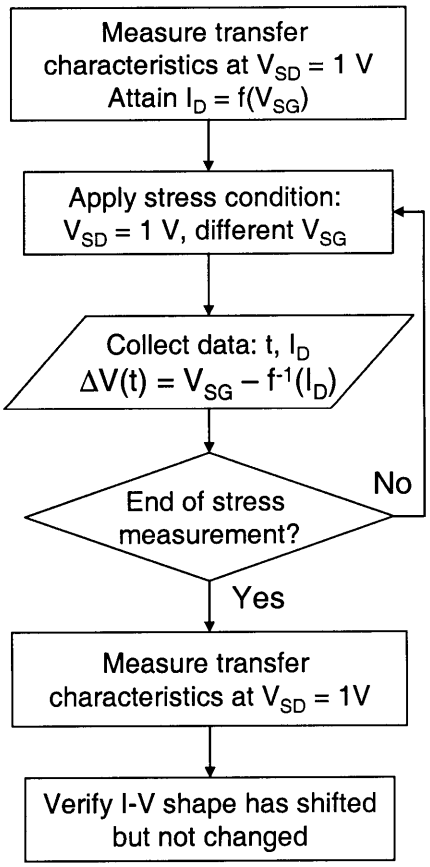

Figure 5-12: Flow chart for measuring ΔV using the on-the-fly stress characterization method.

5.3.1 Stress Time Dependence

The BSE is characterized vs. stress times at different stress V_{SG}'s at 20 °C. Figure 5-13 shows measurements for ΔV using the on-the-fly stress characterization method for one of the stress conditions. The resulting measurement in Figure 5-14 shows that the measured data fits well to the stretched-exponential equation shown below:

$$\Delta V(t) = \Delta V_{FINAL}\{1-\exp(-(t/\tau)^{\beta})\} \quad (5\text{-}3)$$

where t is the stress time, ΔV_{FINAL} is the voltage at which ΔV saturates, and τ and β are fit parameters. The fit parameters to the measurements are given in Table 5-1. The stress V_{SG} is limited to a maximum of 40 V as the effects of gate dielectric breakdown are observed at higher voltages.

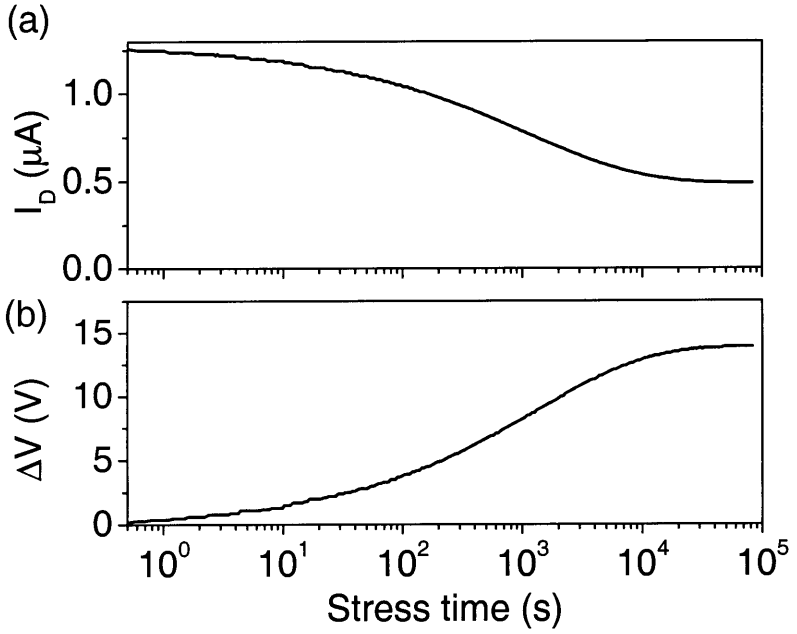

Figure 5-13: (a) The current measurement during stress condition of V_{SG} = 35 V, V_{SD} = 1V at 20 °C, and (b) the extracted ΔV using the on-the-fly stress characterization method.

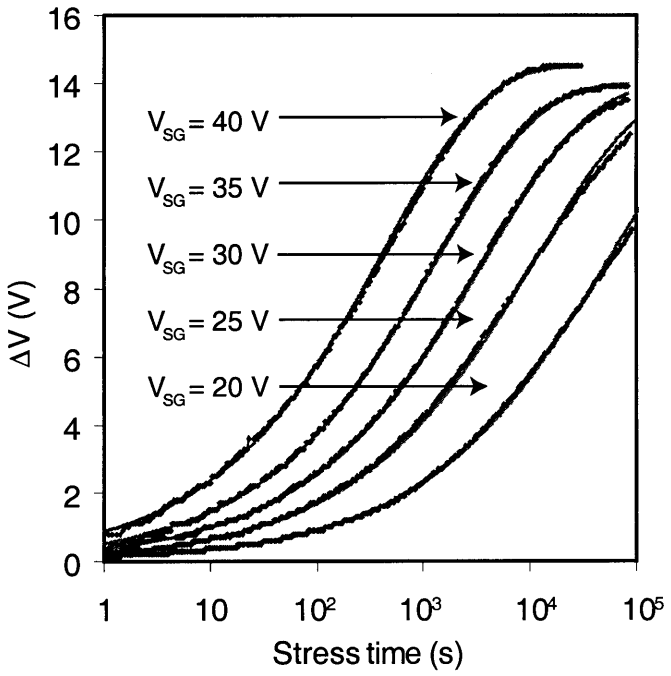

Figure 5-14: Stress time dependence of the induced ΔV for various gate bias-stress conditions. Each stress condition has fifty data points per decade. The solid green lines, representing the stretched-exponential fit made to the data, are plotted on top of the data.

Stress V_{SG} (V)	ΔV_{FINAL} (V)	τ (s)	β
20	14	55000	0.43
25	14	12000	0.43
30	14	3900	0.44
35	14	1400	0.44
40	14.5	440	0.46

TABLE 5-1: FIT PARAMETERS TO DIFFERENT V_{SG} STRESS CONDITIONS IN THE STRETCHED-EXPONENTIAL MODEL

It is notable that the BSE saturates when the current is about 40% of the original current in Figure 5-13. This indicates that the BSE saturates even when there are free carriers left in the channel. This contrasts with the BSE observed for a-Si:H TFTs. In a-Si:H TFTs the BSE only saturates when there are no more carriers in the channel, typically at $\Delta V_{FINAL} = V_{GS} - V_{T0}$ as shown in Figure 5-15. In contrast, ΔV_{FINAL} in pentacene OTFTs is independent of

stress V_{SG} indicating that saturation of the BSE is not due to the limited number of carriers. We propose that this saturation of the BSE in pentacene OTFTs occurs due to exhaustion of trap sites.

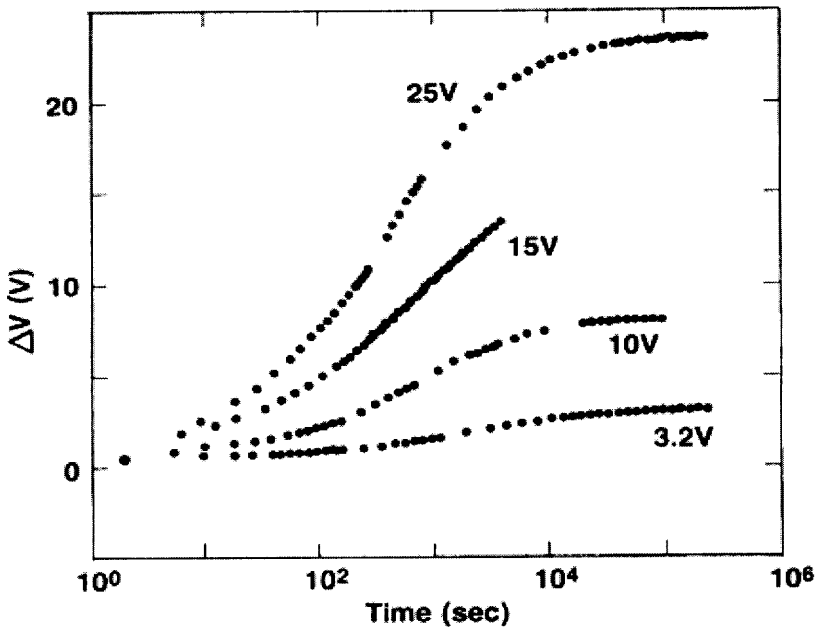

Figure 5-15: The gate voltage shift for a-Si:H TFTs subjected to various stressing voltages indicated vs. time. From [19].

To investigate the effect of limited number of trap sites, the stretched-exponential equation is modeled from a semi-empirical rate equation. The stretched-exponential equation describes the phenomena of a wide class of disordered materials. The form was first observed by Kohlrausch in 1847 [22] in the time-dependent decay of the electric charge stored on a glass surface. The equation can be used to model processes with a distribution of time constants, which is expected in a disordered system.

The stretched-exponential equation results from the slowing of the release rate of the electrons. Kohlrausch showed that this slowing rate constant can be empirically modeled by $k_0 t^{\beta-1}$ where k_0 and β are constants with $0 < \beta < 1$, and t is the time. As time increases the rate constant decreases monotonically. Substituting the rate constant, k, with $\beta k_0 t^{\beta-1}$ in a standard rate process dN/dt = -kN, the following rate equation is obtained:

$$dN/dt = -\beta\, k_0\, t^{\beta-1}\, N \qquad (5\text{-}4)$$

where N is the number of electrons stored on the glass surface. Using separation of variables, and integrating both sides, the following stretched-exponential equation result.

$$\int \frac{1}{N} dN = -\int \beta k_0 t^{\beta-1} dt$$

$$\ln N = -k_0 t^{\beta} + C$$

Taking the exponential on both sides:

$$N = N_0 \exp(-(t/\tau)^{\beta}) \qquad (5\text{-}5)$$

where N_0 is the initial number of electrons, and $1/\tau^{\beta} = k_0$.

To model the BSE using a similar approach, the original rate equation is modified here to account for the fact that both carriers and empty traps are needed for the trapping to occur. To model the trapping process, the following variables are defined:

N (t) = the density of trapped carriers [cm^{-2}]

N_T = the density of traps [cm^{-2}]

p = the initial channel carrier density [cm^{-2}]

N_T and p are fixed with respect to time, and N is a function of stress time. Moreover $p = C_i(V_{SG} - V_{T0})$, where V_{T0} is the initial threshold voltage, and $N(0) = 0$. ΔV can be expressed in terms of N (t), if all the traps are assumed to be at the semiconductor/dielectric interface. In this case:

$$\Delta V = qN/C_i \tag{5-6}$$

In order for carriers to be trapped, there needs to be both a free carrier and an empty trap. The following rate equation can be used in place of Equation (5-4):

$$dN/dt = -\beta\, k_0\, t^{\beta-1}\,(p-N)(N_T-N) \tag{5-7}$$

where k_0 is the rate constant which is a function of the attempt frequency, temperature, and electric field. The implication of the empirical fit parameter β will be considered in detail later. The term in the first bracket in Equation (5-7) is the density of free carriers remaining in the device, and the term in the second bracket is the density of empty traps. The rate of trapping, $\beta\, k_0\, t^{\beta-1}$, decreases with time, which can be physically related to the fact that as the traps with shorter time constants are filled, the time constants associated with the remaining empty traps are longer resulting in a lower trapping rate.

The differential equation can be solved by separation of variables and integrating both sides:

$$\left(\frac{1}{p-N} - \frac{1}{N_T - N}\right) dN = (N_T - p)\beta\, k_0 t^{\beta-1} dt$$

Integrating both sides gives:

$$\left(-\ln(p-N)+\ln(N_T-N)\right)=(N_T-p)k_0t^{\beta}+C$$

Taking the exponential on both sides, and applying N(0) = 0 gives:

$$\frac{N_T-N}{p-N}=\frac{N_T}{p}\exp\left((N_T-p)k_0t^{\beta}\right)$$

Finally solving for N gives:

$$N(t)=\frac{pN_T\left[\exp\left((N_T-p)k_0t^{\beta}\right)-1\right]}{N_T\exp\left((N_T-p)k_0t^{\beta}\right)-p} \tag{5-8}$$

If $p >> N_T$, i.e. there are much more channel carriers than traps, and t is appreciably large, the first term in the denominator becomes negligible and Equation (5-8) approximates to:

$$N(t)=N_T\left[1-\exp\left(-(p-N_T)k_0t^{\beta}\right)\right] \tag{5-9}$$

which is in the form of a stretched-exponential. Recalling that $\Delta V = qN/C_i$ and by comparing Equation (5-9) with Equation (5-3), we can infer that $\Delta V_{FINAL} = qN_T/C_i$ and is independent of V_{SG}. In addition τ in equation (5-3) can be related to the rate of trapping by $1/\tau^{\beta} = (p - N_T)k_0$.

Similarly for $N_T >> p$, Equation (5-8) can be simplified to result in:

$$N(t)=p\left[1-\exp\left(-(N_T-p)k_0t^{\beta}\right)\right] \tag{5-10}$$

which is also in the stretched-exponential form, but $\Delta V_{FINAL} = qp/C_i$ and now depends on the channel carrier density, p. $p = C_i(V_{SG} - V_{T0})/q$, and thus $\Delta V_{FINAL} = (V_{SG} - V_{T0})$. In addition τ in equation (5-3) can be related to the rate of trapping by $1/\tau^{\beta} = (N_T - p)k_0$.

For the measured OTFTs at stress V_{SG} ranging from 20 V to 40 V, $p > N_T$. Therefore, the ΔV saturates at 14 V independent of the V_{SG} because the traps are exhausted before the channel carriers. Using the measured $C_i = 15$ nF/cm^2, N_T can be calculated as $N_T = C_i\Delta V_{FINAL}/q$. The calculated N_T is 1.3 x 10^{12} cm^{-2} for the measured ΔV_{FINAL} of 14 V. This value of N_T is reasonable considering that interface states in MOSFETs are in the range of $10^9 - 10^{12}$ cm^{-2} [23]. The calculated NT is also reasonable considering that the density of pentacene molecules at the interface is about 10^{14} cm^{-2} [24], indicating that the density of defects is less than the density of molecules at the interface. It is difficult to compare N_T with results from other TFTs as this is the first report of ΔV_{FINAL} that is independent of V_{SG}. However the β and τ values ($\beta \sim 0.43$, $\tau \sim 10^5$ s) from this work are similar to those reported from other pentacene transistors [21] ($\beta \sim 0.4$, $\tau \sim 10^4$ s), [25] ($\beta \sim 0.28$, $\tau \sim 10^4$ s) give confidence in the measurement.

Equation (5-10) predicts two observable characteristics for stress $V_{SG} < 14$ V ($p < N_T$). First, $\Delta V_{FINAL} = V_{SG} - V_{T0}$. Secondly, the dependence of τ on V_{SG} will be drastically reduced. When $p < N_T$, $1/\tau^{\beta} = (N_T - p)k_0$. $N_T - p$ decreases as V_{SG} increases offsetting k_0 increase as V_{SG} increases and results in τ that depends less on V_{SG} compared to the $V_{SG} > 14$ V ($p > N_T$) region. The k_0 increases with V_{SG} because the barrier for carrier trapping is lowered with increasing electric field.

To verify these two characteristics predicted by the model for the case where $p < N_T$, stress measurement are performed below $V_{SG} = 14$ V. First, the transistor is stressed until the ΔV is saturated at $V_{SG} = 10$ V. Because it was going to take more than a month to measure ΔV saturating at 20 °C, accelerated stress test was performed at 50 °C. The measurement in Figure 5-16 verifies that the BSE saturates when there are no more carriers in the channel at $V_{SG} - V_{T0}$, with V_{T0} at 1 V as extracted in Figure 4-4.

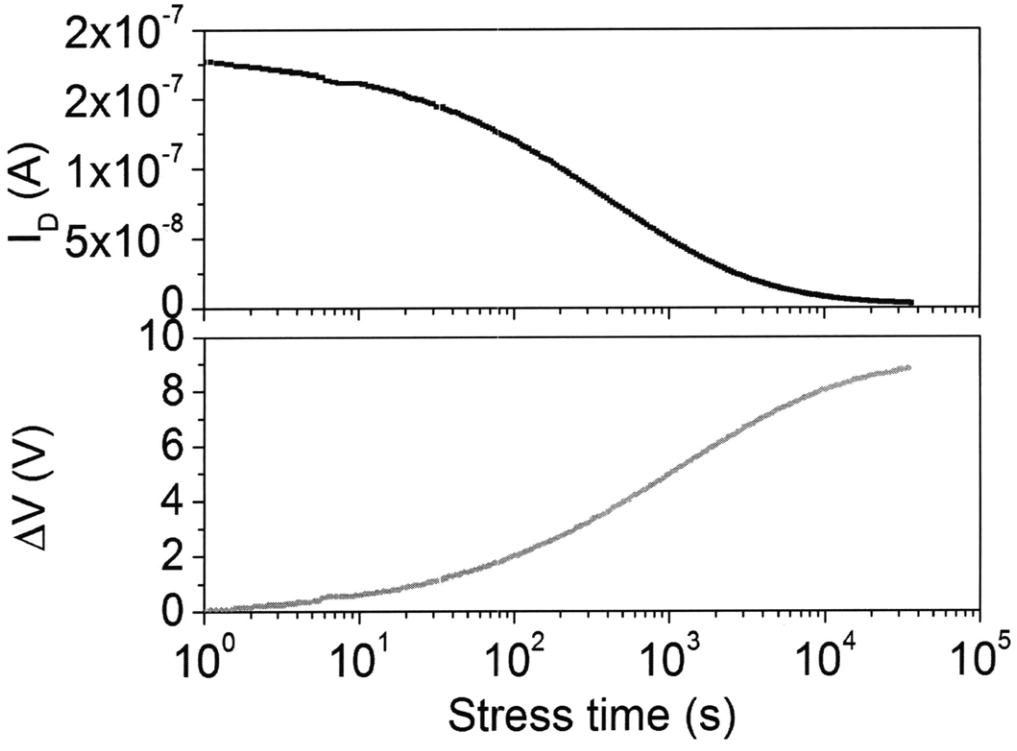

Figure 5-16: Accelerated stress measurement at $V_{SG} = 10$ V, $V_{SD} = 1$ V, and 50 °C.

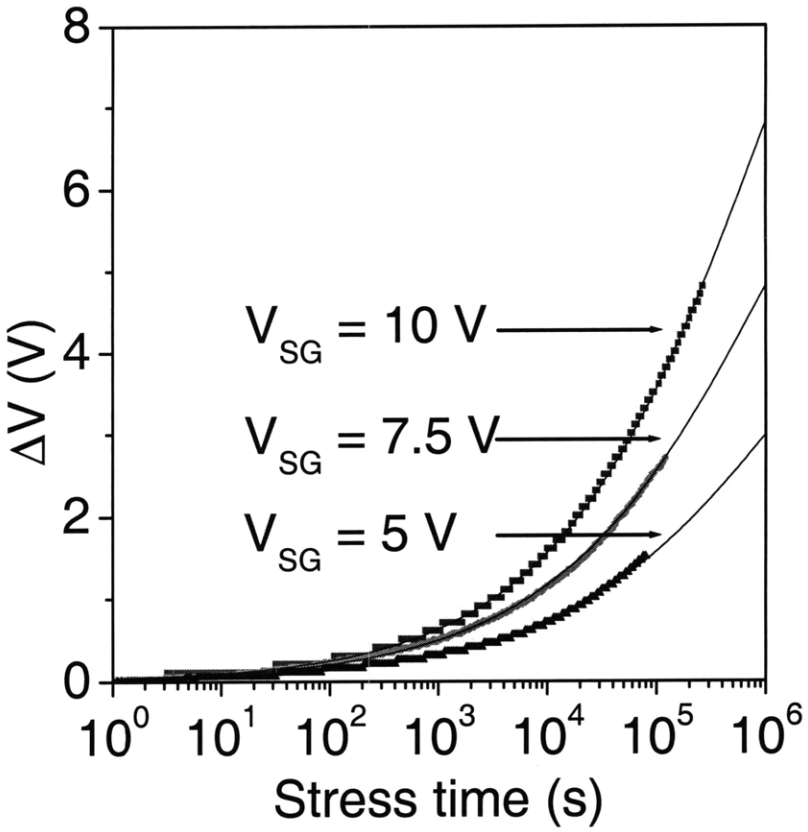

Figure 5-17: Stress time dependence of the induced ΔV for various gate bias-stress conditions. Each stress condition has fifty data points per decade. The solid lines, representing the stretched-exponential fit made to the data, are plotted on top of the data.

Stress V_{SG} (V)	ΔV_{FINAL} (V)	τ (s)	β
5	4	6.4×10^5	0.39
7.5	6.5	6.0×10^5	0.40
10	9	5.2×10^5	0.42

TABLE 5-2: FIT PARAMETERS TO LOW V_{SG} STRESS CONDITIONS IN THE STRETCHED-EXPONENTIAL MODEL

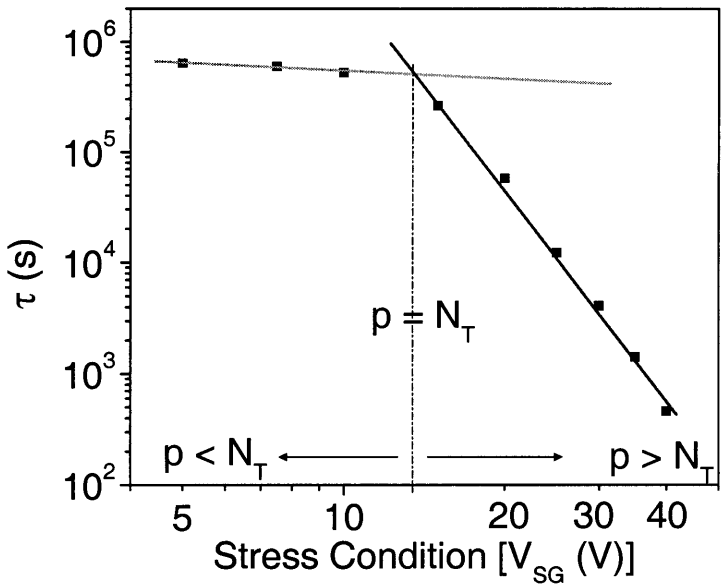

Figure 5-18: The plot of τ vs. V_{SG} for both $p < N_T$ and $p > N_T$ region. τ drops precipitously with increasing V_{SG} above 14 V ($p = N_T$).

Next, stress measurements are performed at V_{SG} = 5, 7.5, 10 V at 20 °C to find the τ dependence on V_{SG}. The measurement results are shown in Figure 5-17 and the fit parameters for the stretched-exponential fit are summarized in

Table 5-2. As shown in Figure 5-18, when τ is plotted against V_{SG}, a dramatic change in the dependence of τ is seen with respect to V_{SG} below 14 V, as predicted by our model.

Modeling

In the previous section, the time dependence of the BSE is explained from a simple rate equation. Although the rate equation approach is useful in understanding the effects of the limited number of traps, the physical meaning of β and τ is not explained by this approach as it is semi-empirical. To gain a fundamental understanding of the stretched-exponential equation, it is approached theoretically. As noted above, the stretched-exponential equation

results from dispersion of time constants due to the disorder in the material. The dispersion of time constants can be modeled by a combination of individual traps each having its own trapping time constant, τ_{trap}, that describes how the traps will be occupied by holes as a function of stress time, t:

$$N_{\tau trap} = D_T(\tau_{trap})\left((1 - \exp(-t/\tau_{trap})\right) \quad (5\text{-}11)$$

where $N_{\tau trap}$ is the density of trapped carriers in traps with τ_{trap}, and $D_T(\tau_{trap})$ is the density of trap states (DOS) at τ_{trap}. The BSE response of the combination of all the traps with different τ_{trap} can be expressed as:

$$N(t) = \sum_{\tau_{trap}} D_T(\tau_{trap})\left((1 - \exp(-t/\tau_{trap})\right) \quad (5\text{-}12)$$

where N(t) is the total density of trapped carriers and t is the stress time. Σ is used instead of integration because calculation is done in discrete space. Modeling the N(t) as a linear combination of exponential functions, allows us to extract $D_T(\tau_{trap})$ from the ΔV vs. t data. The extraction of the $D_T(\tau_{trap})$ is performed by optimally fitting the data with an assumed DOS. This approach has been successfully used in analyzing the trap states that cause current degradation in GaN high electron mobility transistors [26].

To first validate the DOS extraction tool, it is tested against simulated data that is generated from a known log-normal distribution of $D_T(\tau_{trap})$. The simulated data is calculated from

Equation (5-12). The simulated data is then input into the DOS extraction tool and the extracted DOS is compared with the original $D_T(\tau_{trap})$. The extracted DOS closely matches the input DOS as shown in Figure 5-19 verifying that the extraction tool can accurately extract $D_T(\tau_{trap})$. The *MATLAB* code used for DOS extraction is available in Appendix C.

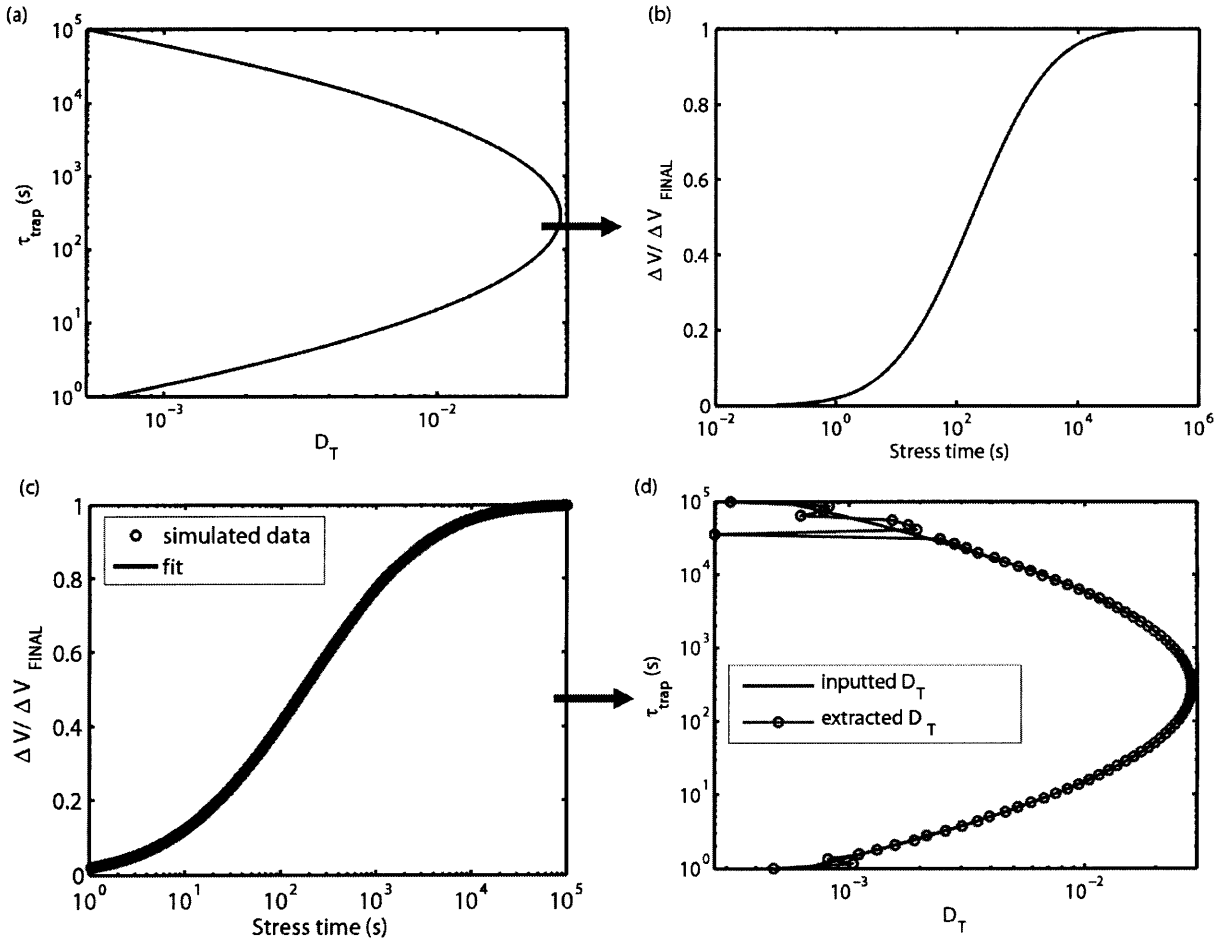

Figure 5-19: Verification of the DOS extraction tool. (a) The log-normal distribution of DOS which is used to generate simulated data in (b) according to Equation (5-12). (c) The DOS extraction tool finds the optimal DOS that fits the simulated data best. Both simulated data and the fit are shown. (d) The extracted DOS match the input DOS well indicating that DOS can be correctly extracted from the extraction tool.

To understand the meaning of β and τ in the stretched-exponential equation, the stretched-exponential equation with different β and τ are input into the DOS extraction tool. Figure 5-20 shows the DOS extracted from two stretched-exponential responses with identical τ's, but different β's. The lower β yields DOS which is more dispersed. The peak DOS of lower β is also lower because the DOS, which add up to one, is spread out over a larger range of τ_{trap}. In the extreme case when $\beta = 0$, the DOS will be dispersed through infinite range of τ_{trap}. In the opposite extreme when $\beta = 1$, all the traps will have the same time constant, and the stretched-exponential equation turns into a simple exponential equation with a single time constant. Therefore β determines the dispersion of τ_{trap}, with lower β meaning more dispersion.

In Figure 5-20 (a), the two stretched exponential responses cross at the point when t = 1000 s and 63% of the traps are filled. This can be explained from the mathematical form of the stretched exponential equation; when $t = \tau$, $1 - \exp(-t/\tau)^{\beta} = 1 - \exp(-1) = 0.63$ regardless of β. Therefore, in stretched exponential response, τ is always the time when 63% of the traps are filled and it can be considered effectively as a median trapping time constant. Although in a strict sense it is the 63 percentile trapping time constant, we will refer to it as the median trapping time constant for simplicity.

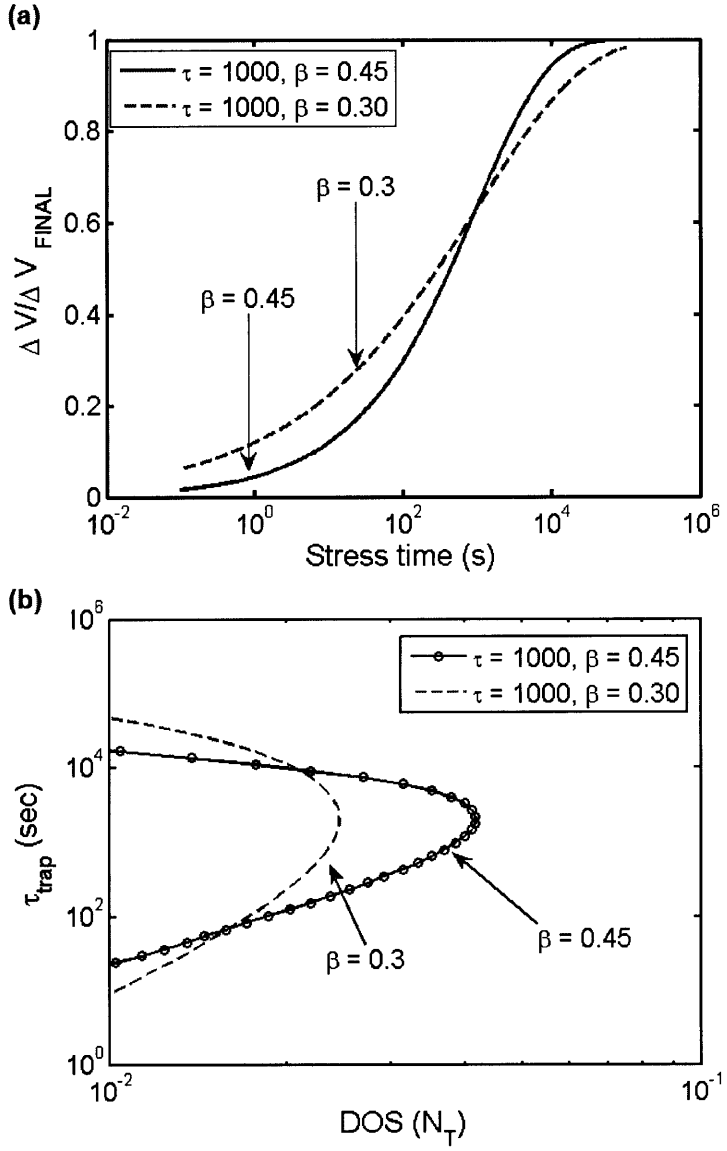

Figure 5-20: (a) Plot of two stretched-exponential responses with different β. (b) Plot of the extracted DOS from the two stretched-exponential equations. DOS with lower β is more dispersed.

Next the effect of τ on the dispersion of τ_{trap} is explored. Figure 5-21 shows the DOS from two stretched-exponential responses with different τ's. It illustrates that the shape of the DOS does not change with τ; only the median τ_{trap} changes.

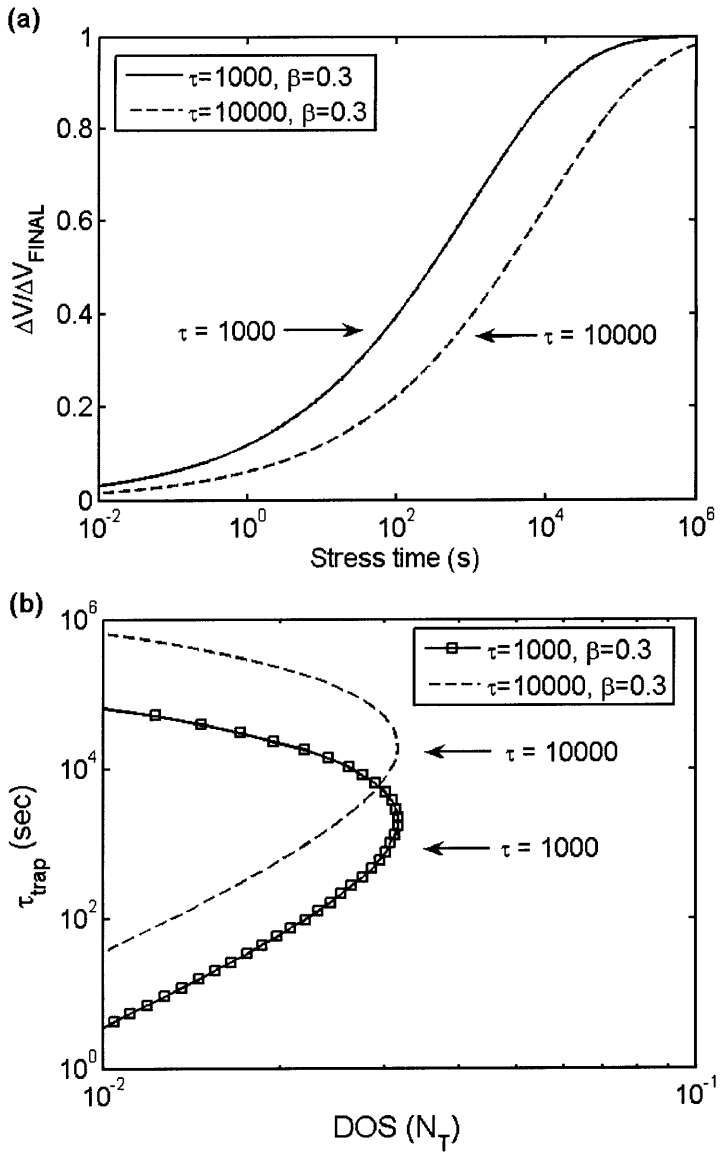

Figure 5-21: (a) Plot of two stretched-exponential responses with different τ. (b) Plot of the extracted DOS from the two stretched-exponential equations. The shape of the DOS is not changed. The two DOS' are offset by an order of magnitude of τ_{trap}.

It is notable that τ_{trap} can be as long as hundreds of thousands of seconds. Such a long trapping time constant indicates that the trapping process is not a conventional one where the carrier simply traps when it reaches the vicinity of a trap within the capture-cross section. Instead, there is an energy barrier for a carrier to trap. The nature of this barrier is disordered

as evidenced by the dispersion of trapping time constants. With the presence of a barrier to trap, the trapping time constant can be modeled as the following:

$$\tau_{trap} = \nu_0^{-1} \exp(E_B/kT) \tag{5-13}$$

where ν_0 is a constant that is independent of the temperature, and E_B is the energy barrier that the carrier must hop over in order to access the trap. E_B is different for each trap due to the disorder and results in the dispersion of time constants. The energy barrier, E_B, drops as V_{SG} increases attributed to the barrier lowering due to the electric field and can explain the faster BSE as V_{SG} increases. The dispersion of τ_{trap} can be explained by the disorder in the material that leads to a different E_B for each trap. In the following section, E_B is investigated by changing the temperature.

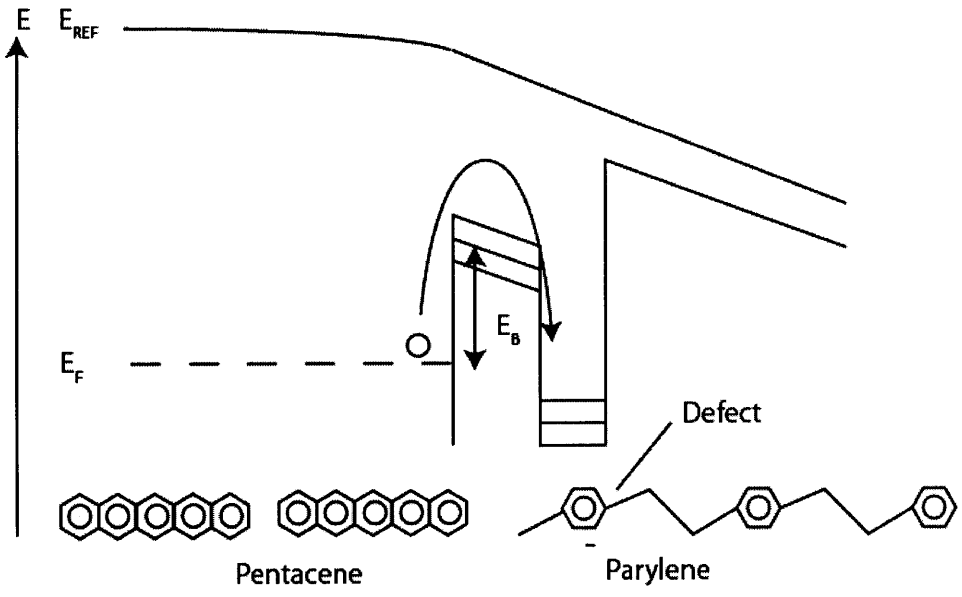

Figure 5-22: An example trapping mechanism. The carrier must hop over a barrier in order to access the traps, which in this case are dangling bonds in the parylene. The energy barrier as well as the energy level of the trap is dispersed due to the disorder in the material.

5.3.2 Temperature Dependence

The ΔV dependence on temperature was investigated by measuring the BSE at different temperatures from 0 °C to 40 °C while keeping the stress V_{SG} and V_{SD} constant at 35 V and 1 V, respectively. Figure 5-23 shows the measurement results, and Table 5-3 summarizes the fit parameters for the stretched-exponential equation. The table shows that τ increases while β decreases with decreasing temperature.

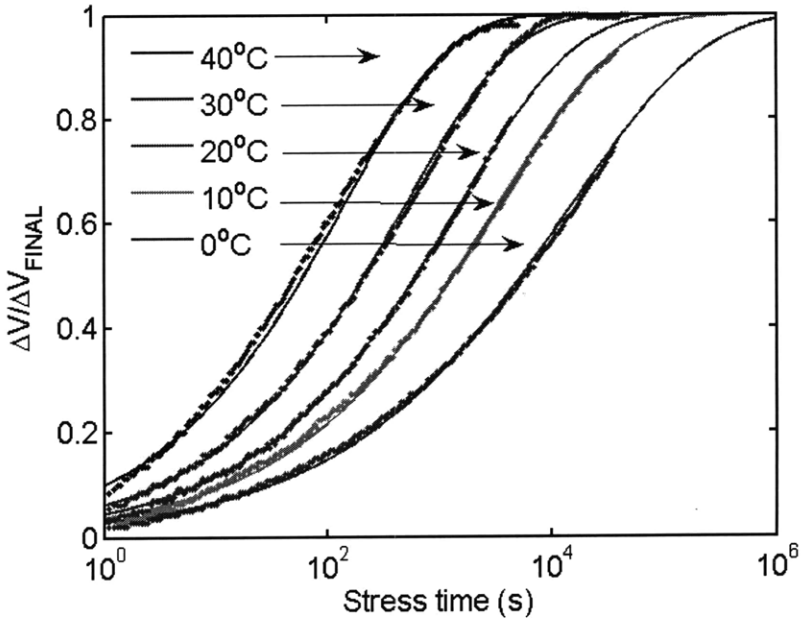

Figure 5-23: Stress measurements at different temperatures. V_{SG} = 35 V, V_{SD} = 1 V is applied for bias stress. Measurement results are shown in dots and the fits to the stretched-exponential equation are shown in solid lines.

Temperature	ΔV_{FINAL} (V)	τ (s)	β
40 °C	14	138	0.46
30 °C	14	460	0.45
20 °C	14	1500	0.42
10 °C	14	3300	0.40
0 °C	14	15000	0.37

TABLE 5-3: FIT PARAMETERS TO DIFFERENT TEMPERATURE STRESS DATA TO THE STRETCHED-EXPONENTIAL EQUATION

To explain the temperature dependence of the various parameters, the τ_{trap} introduced in the previous section is utilized. From Equation (5-13), we can predict the τ_{trap} from a given DOS vs. E_B for different temperatures. At lower temperatures, 1/kT in the exponential will be larger resulting in a wider range of τ_{trap} from the same range of E_B. The wider range of τ_{trap} results in more dispersed time constants and lead to lower β and a higher τ as illustrated in Figure 5-24. This explains what is observed for the extracted parameters in Table 5-3.

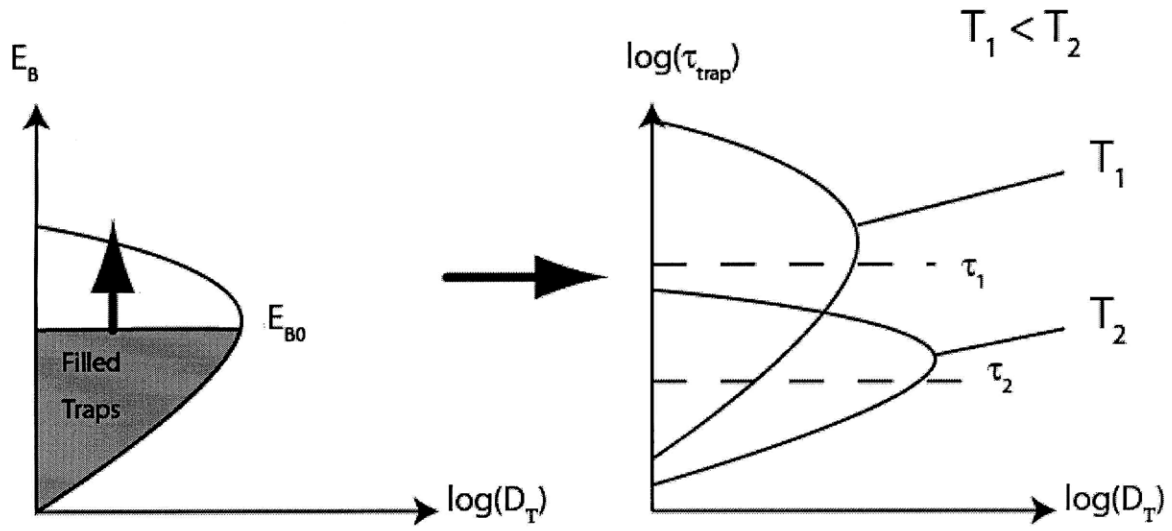

Figure 5-24: Illustration of the relationship between DOS vs. E and DOS vs. τ_{trap} at different temperatures. A single DOS vs. E can lead to different DOS vs. τ_{trap}. In the illustration, the temperature T_1 is less than T_2, and the DOS for T_1 is more dispersed than DOS for T_2 because the DOS is spread over a large range of τ_{trap} resulting in lower β and higher τ for T_1.

As illustrated in Figure 5-24, the traps with the lower energy barrier will fill first because the energy barrier exponentially increases the τ_{trap}. For example, by the time trap states at E_{B0} are filled, all the traps below it are filled as well. The order in which the traps are filled is preserved at different temperatures and thus the stress time associated with inducing the same amount of ΔV can be used to extract the related trap energy barrier. For example, the energy

barrier for a trap that is filled when $\Delta V = 1V$ is simply the activation energy of the stress time to induce $\Delta V = 1$ V with respect to different temperatures. As the traps fill, it is expected that the energy barrier associated at different ΔV will increase if the larger time constant is caused by the increase in the energy barrier. The energy barrier at different levels of ΔV is extracted from an Arrhenius plot of stress times to induce the ΔV as shown in Figure 5-25.

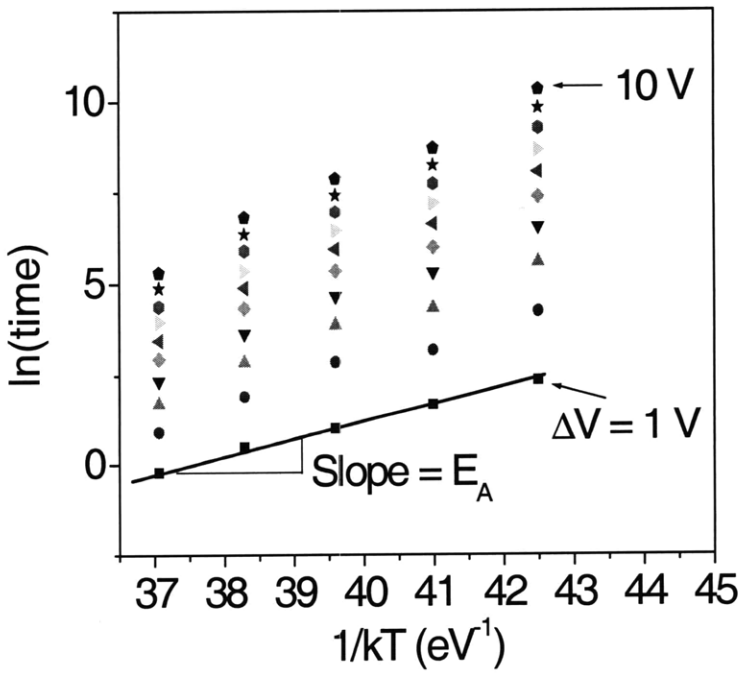

Figure 5-25: Arrhenius plot for extraction of activation energy as a function of ΔV. From the measured stress data in Figure 5-23, the time to reach a fixed ΔV is measured and plotted for each temperature. The activation energy is extracted from the slope of the linear fit to the data as illustrated for $\Delta V = 1$ V.

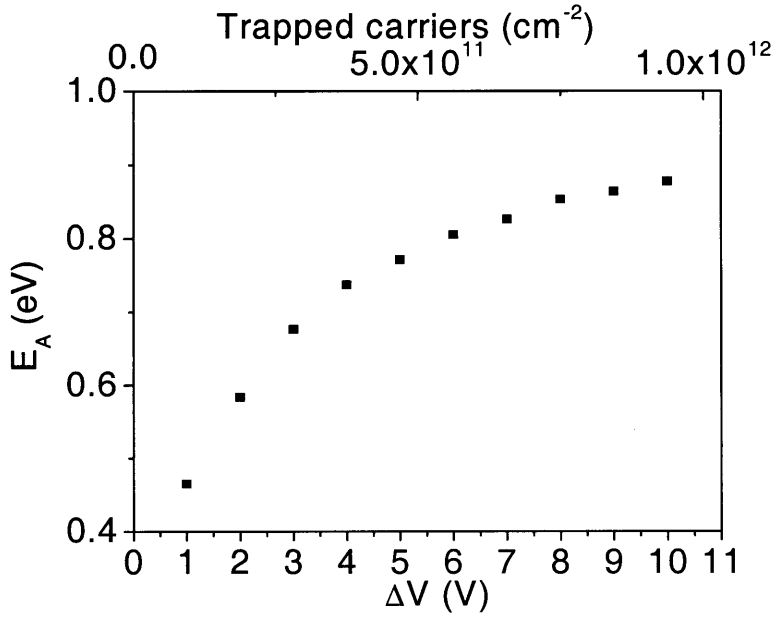

Figure 5-26: The activation energy of the bias-stress time to induce ΔV. The activation energy is the energy barrier associated with the trap that fills at different levels of ΔV. The density of trapped carriers is calculated from the measured ΔV and labeled on the top axis.

As expected, the energy barrier increases as the traps are filled indicating that longer τ_{trap} are indeed associated with higher E_B. The increasing rate of the energy barrier slows as the traps are filled indicating that there are more traps with higher energy barrier, consistent with the shape of the extracted DOS in the previous section.

The DOS is extracted from the measurements in Figure 5-23 by fitting a linear combination of exponentials as introduced in the previous section. With the data measurements from different temperature, the τ_{trap} is converted into E_B by using the relationship given in Equation (5-13). Solving for E_B from Equation (5-13) results in:

$$E_B = kT\{ \ln(\tau_{trap}) + \ln(\nu_0) \} \quad (5\text{-}14)$$

We assume that $\nu_0 = 10^{12}$ Hz which is on the order of phonon vibration and attempt-to-hop frequency [27,28]. The DOS is replotted with respect to E_B as shown in Figure 5-27. The convergence of the DOS indicates that ν_0 is in the correct range. If $(\ln(\nu_0))$ is too large, E_B extracted from τ_{trap} measurements at higher temperatures will be higher because the terms in the brackets are multiplied by kT. Vice versa, if $(\ln(\nu_0))$ is smaller than what it should be, the E_B extracted from higher temperatures will be smaller. Either case, the DOS vs. E_B extracted from different temperature measurements will not overlap. The resulting DOS peak around 0.85 eV is in good agreement with the actual measured activation energy. This agreement achieved with the use of physically likely value of ν_0 gives confidence in the model.

In the literature, values of the activation energy of τ are commonly reported for BSE measurements [29,30,31]. For the measured OTFTs, the activation energy of τ is found to be 0.8 eV. The meaning of this activation energy is explained in the following. Since τ is found to be the median trapping time constant, τ_{trap}, and τ_{trap}'s are exponentially dependent on the energy barriers, the activation energy of τ is the median energy barrier. This relationship between the median τ_{trap} and the median E_B can be further illustrated from Equation (5-13) reproduced below:

$$\tau_{trap} = \nu_0^{-1} \exp(E_B/kT) \quad (5\text{-}15)$$

Because the trapping time constant, τ_{trap}, is exponentially dependent on E_B, τ_{trap} monotonically increases as E_B increases. Therefore, ordering the τ_{trap}'s from the shortest to

the longest would result in the ordering of the corresponding E_B's from the smallest to the largest. As a result, the median trapping time constant will be associated with the median energy barrier in a distribution of energy barriers.

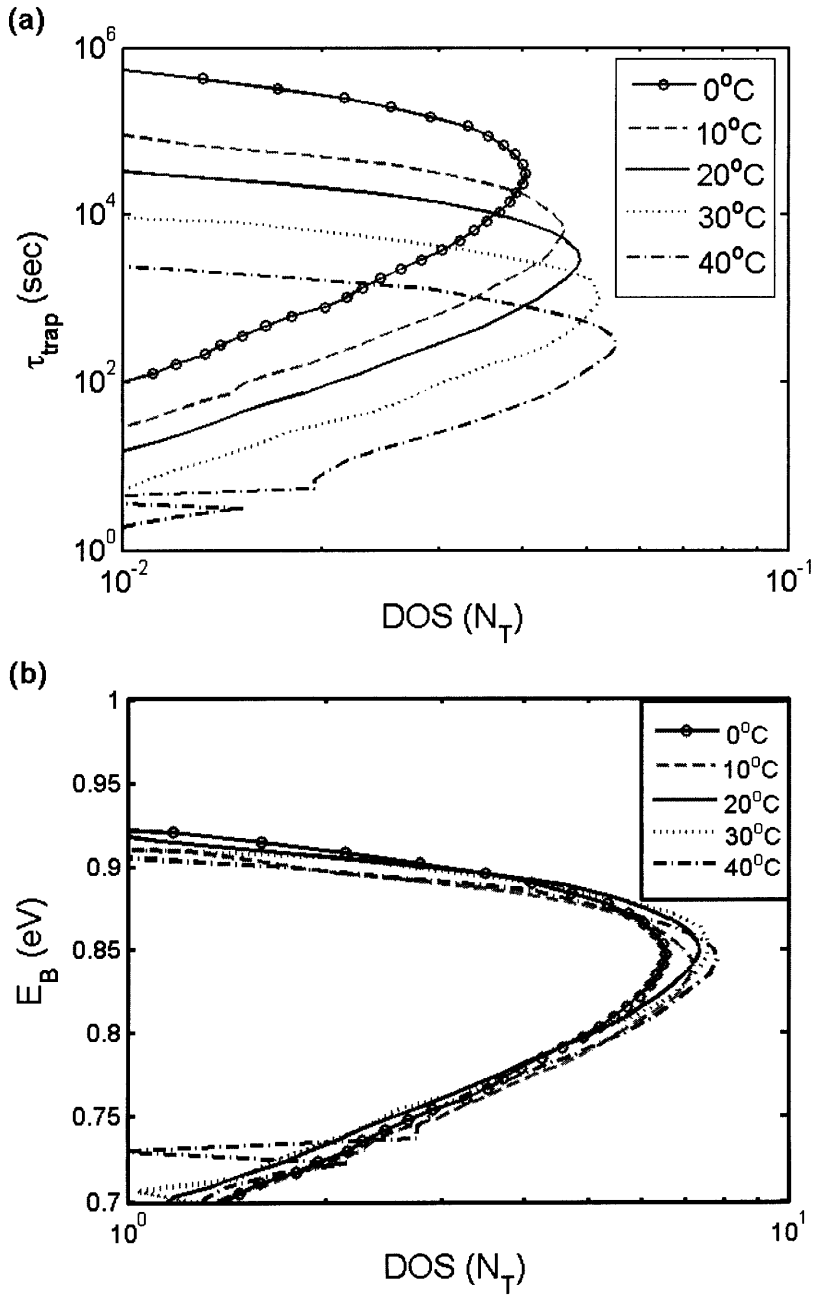

Figure 5-27: Extracted DOS from different temperature stress measurements from Figure 5-23. (a) As a function of time constants. (b) As a function of energy barrier. The extracted DOS matches one another indicating that the trapping at different temperature can be predicted by a single DOS distribution with respect to energy.

5.4 Simplified Expression of the Bias-stress Effect for Simulators

In this section, dependencies of the BSE on stress time and V_{SG} are put together for circuit simulators. First, the dependency of τ in the stretched-exponential equation on V_{SG} must be expressed in terms of V_{SG}. To achieve this goal, τ vs. V_{SG} is plotted on a log-log scale in Figure 5-28. By using $\tau = aV_{SG}^{\alpha}$ where $a = 5.3 \times 10^{13}$ sV^{α}, $\alpha = 6.9$, an adequate fit can be made. With this knowledge, Equation (5-3) can be modified so that $\Delta V(t)$ can be expressed as an explicit function of V_{SG}:

$$\Delta V(t) = \Delta V_{FINAL}\{1-\exp(-(t/aV_{SG}^{-\alpha})^{\beta})\} \qquad (5\text{-}16)$$

where a, α, and β are independent of V_{SG}. Equation (5-16) is used to produce the solid line in Figure 5-29, which plots ΔV after 100 s of stress at different stress V_{SG}. To verify if this equation can be used for multiple devices, measurements on multiple devices are also plotted. The figure shows that equation (5-16) can make reasonable prediction of ΔV for many different devices enabling its use in simulators.

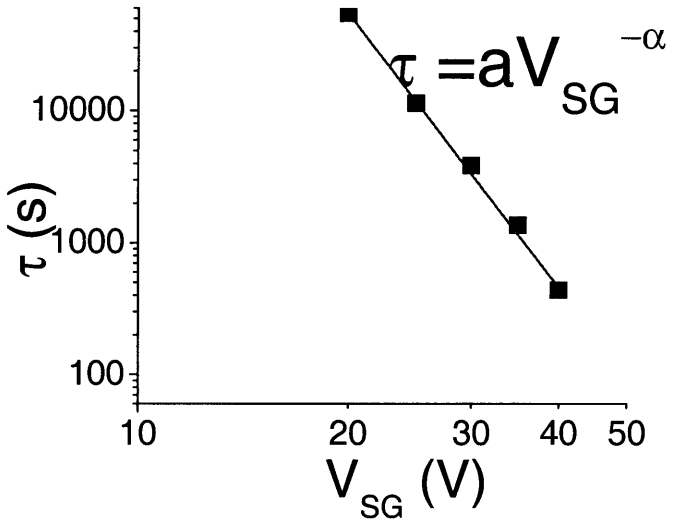

Figure 5-28: Log-log plot of τ vs. V_{SG}. τ for the stretched-exponential equation can be modeled by $\tau = aV_{SG}^{-\alpha}$.

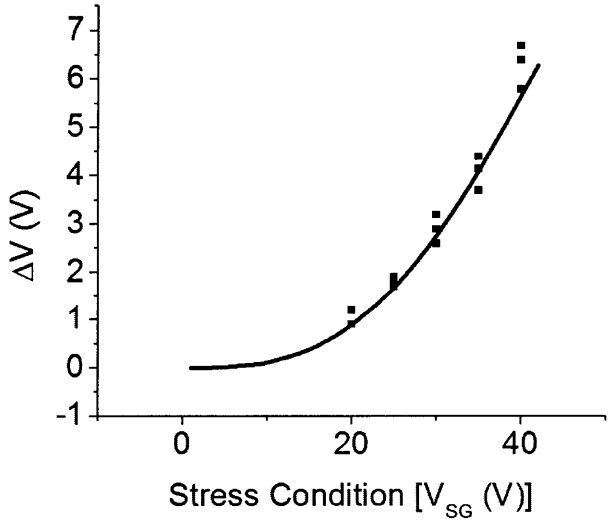

Figure 5-29: ΔV vs. stress V_{SG} at t = 100 s. The V_{SD} during stress was held at 1 V. Each stress condition is repeated three times, each time on a fresh device. The solid line is ΔV predicted by Equation (5-16).

In the case $t << \tau$, the stretched exponential equation can be approximated to the following equation by using $\exp(-x) \approx (1 - x)$ when $x << 1$:

$$\Delta V = \Delta V_{FINAL}\{1 - \exp(-(t/\tau)^{\beta})\}$$

$$\approx \Delta V_{FINAL}\{1 - (1 - (t/\tau)^{\beta})\}$$

$$= \Delta V_{FINAL}(t/\tau)^{\beta}$$

Plugging in $\tau = aV_{SG}^{-\alpha}$ to the above equation,

$$\Delta V = \Delta V_{FINAL}(t/a)^{\beta} V_{SG}^{\alpha\beta} \qquad (5\text{-}17)$$

The resulting equation is in the same form as Equation (5-1) where $n = \alpha\beta$. The n calculated from the extracted α and β (6.9 and 0.44) is 3, and closely matches the extracted n of 2.8 in Section 5.2.2. In addition, Equation (5-17) can be rewritten as:

$$\Delta V = (\Delta V_{FINAL}/a^{\beta}) V_{SG}^{n} t^{\beta} \qquad (5\text{-}18)$$

Therefore for short stress times, the stretched-exponential equation can be approximated by power law dependence on stress time, with $\Delta V \sim t^{\beta}$. The V_{SD} dependence can be worked into Equation (5-17) by using the previously found V_{SD} dependence in Section 5.2.2:

$$\Delta V = (Q/Q_0)(\Delta V_{FINAL}/a^{\beta}) V_{SG}^{n} t^{\beta} \qquad (5\text{-}19)$$

where Q is defined in Equation (5-2), and $Q_0 = C_i(V_{SG} - V_{T0})$.

5.5 Implications to Circuit Lifetime

The BSE under different bias-stress conditions have been studied in the previous sections. With the data gathered in the previous sections, this section aims to find the implications of the BSE to circuit lifetime.

Our immediate insight is to lower the operating voltage because the BSE is strongly dependent on the V_{SG} during operation. For example, operating the OTFT at 20 V instead of 30 V will increase the half-life, defined as the operation time in which current is half of its initial value, to 12600 s from 4600 s. A device with higher W/L can be used to compensate for the decreased current due to lower V_{SG}. We find that in some applications, particularly where the tolerance to ΔV scales linearly with the operating voltage, there is a critical voltage which the operating voltage should be kept below for optimal circuit lifetime.

First, a worst-case approximation is considered. In this case, the critical transistor is assumed to be always under stress with the maximum stress voltage applied in the linear region. For a circuit with V_{DD} power supply, the $V_{SG} = V_{DD}$, and $V_{SD} = 1$ V is assumed. Under these conditions, two scenarios can be considered.

- Lifetime is determined by the critical transistor reaching $\Delta V = 1$ V regardless of V_{DD}.
- Lifetime is determined by the critical transistor reaching $\Delta V/V_{DD} = 10\%$.

The first case can be related to an opamp input transistor failing because the offset voltage is higher than specification, and the second case can be related to an inverter where the noise margin scales with V_{DD} and fails if noise margin becomes negative due to too much ΔV.

For the two scenarios the circuit lifetime can be estimated from the measured data for different V_{DD}. This is a lower bound estimation as the V_{SG} will not always be at V_{DD}, and V_{SD} can also increase to be in the saturation region where the BSE is less. However, this will serve as a good engineering guideline. The result is shown in Figure 5-30 and Figure 5-31. In both scenarios, the lifetime decreases with increasing V_{DD} and the lifetime decreases more rapidly above the point where $p = N_T$, or $V_{SG} - V_{T0} = 14$ V. This change in rate is especially large for the case when the lifetime is determined by critical ΔV that scales with V_{DD}. Hence the V_{DD} should be kept below this point for circuits with these lifetime restrictions.

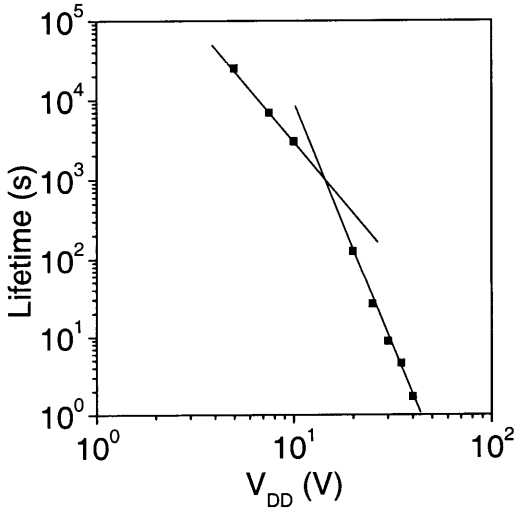

Figure 5-30: The circuit lifetime calculated for the case where circuit lifetime threshold is $\Delta V = 1$ V.

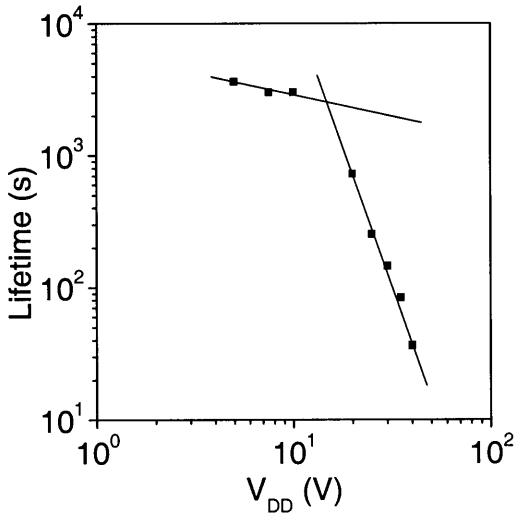

Figure 5-31: The circuit lifetime calculated for the case where circuit lifetime threshold is $\Delta V/V_{DD} = 10\%$.

In actual applications the lifetime will be longer because the critical device will not always be biased at V_{DD}. The lifetime of the circuit will increase because the total stress time is reduced, and the recovery of the BSE will take place when the transistor is off. To get an idea of how much improvement this effect will have, the gate of the transistor is pulsed with 20 V every 500 ms with 50% duty cycle for an extended length of time. Using the same criteria as before, the lifetime of the circuit in this practical case is longer by 50 times than estimated through worst-case approximation.

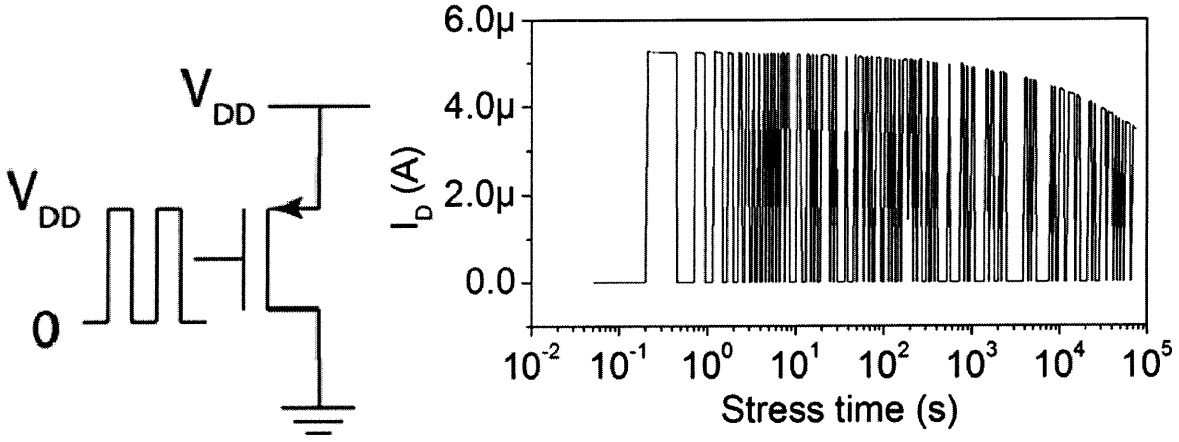

Figure 5-32: Pulsed gate measurements. V_{DD} = 20 V.

	$\Delta V = 1V$	$\Delta V/V_{DD} = 10\%$
DC (s)	130	720
Pulsed (s)	7200	36000

Table 5-4: Lifetime measurements for V_{DD} = 20 V when the gate is stressed with a DC bias, and pulsed gate bias. The lifetime from the pulsed gate bias is 50 times longer in both scenarios of circuit lifetime calculations.

5.6 **Summary**

The BSE causes operational instability in TFTs which limits the technology from being used in a wide range of applications. To understand the electrical characteristics of the BSE in OTFTs applicable to large-area flexible electronics, we systematically studied it on integrated pentacene OTFTs fabricated at MIT.

The stress was characterized in terms of ΔV using two different measurement methods. The dependencies on various stress conditions were thoroughly studied. From the measurements, we learned that the BSE is caused by trapping of the channel carriers and is fully reversible at room temperature. Both field and carriers are required for the BSE, and the current is not a direct cause of the BSE.

The time dependence of the BSE is found to be well modeled by the stretched-exponential equation which can arise in disordered systems due to dispersion of time constants. One interesting observation from the measurements is that the BSE seems to saturate even when there is a high concentration of free carriers in the channel. We propose that the saturation of the BSE is caused by the exhaustion of trap sites in the channel. A simple rate equation is developed based on this assumption and from this model we successfully predicted and verified the behavior of the BSE for low stress V_{SG} in terms of ΔV_{FINAL} and τ dependence on V_{SG}.

To further understand the physical meaning of the fit parameters τ and β, the stretched-exponential equation was theoretically studied using a DOS extraction tool in *MATLAB*. From the study, it is found that τ is the average time constants for trapping, and β is related to the dispersion of the time constants, with higher β indicating less dispersion. To understand if the source of dispersion is an energetic barrier, temperature measurements were performed. The measurements indicate that indeed the change in the time constants and dispersion can be aptly modeled by dispersion in energy barrier .

Next, attention was turned to the application of measured data to simulate the BSE in circuit applications and estimating the circuit lifetime due to the BSE. The dependence of τ on the V_{SG} is derived and an equation that expresses ΔV in terms of V_{SG}, V_{SD}, and the stress time is derived and verified for use in simulations. For circuit lifetime, we found that for there is a severe trade off between circuit lifetime and operational V_{SG}, once the V_{SG} increases above a critical voltage. This critical voltage is found to be the voltage when the V_{SG} induces more carriers in the channel than trap sites. It is recommended that OTFT circuits are designed below this critical voltage for optimal circuit lifetime.

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Chapter 6

Recovery of the Bias-stress Effect

Recovery of the BSE has been observed in OTFTs as soon as the bias stress is removed [1,2,3]. In this chapter, the recovery is investigated to understand more about the BSE. The temperature dependence and the field dependence of the recovery are studied. In addition, the location of the traps is investigated.

Prior to this work, only qualitative study has been performed on the recovery. Street *et al.* have reported [2] that devices generally recover within 0.5 V of the original threshold voltage in a polymer OTFT. The recovery has been reported to be temperature activated and depend on how long the device has been stressed. Generally, the recovery time is proportional to the device stress time. However such a result is not conclusive as the stress time was excessive (140 days) and the difference may have stemmed from the changed device characteristics over that time. Mathijssen *et al.* have reported complete recovery in another polymer OTFT, with time constants similar to the BSE [3].

Recovery from the BSE is observed for pentacene OTFTs used in this work as well. In a transistor that has been stressed for a hundred seconds, a complete recovery of the BSE was measured in a day after storage in nitrogen ambient at room temperature as shown in Figure 6-1. Transistors that had been stressed for a longer period of time have also been observed to recover the original I-V characteristics. Figure 6-2 shows I-V characteristics before the stress, after the stress, and after one to two months in nitrogen box at room temperature. Complete recovery of the original I-V characteristics is observed for all the stressed transistors. It should be noted, however, devices that have been stressed for a longer time took longer to recover.

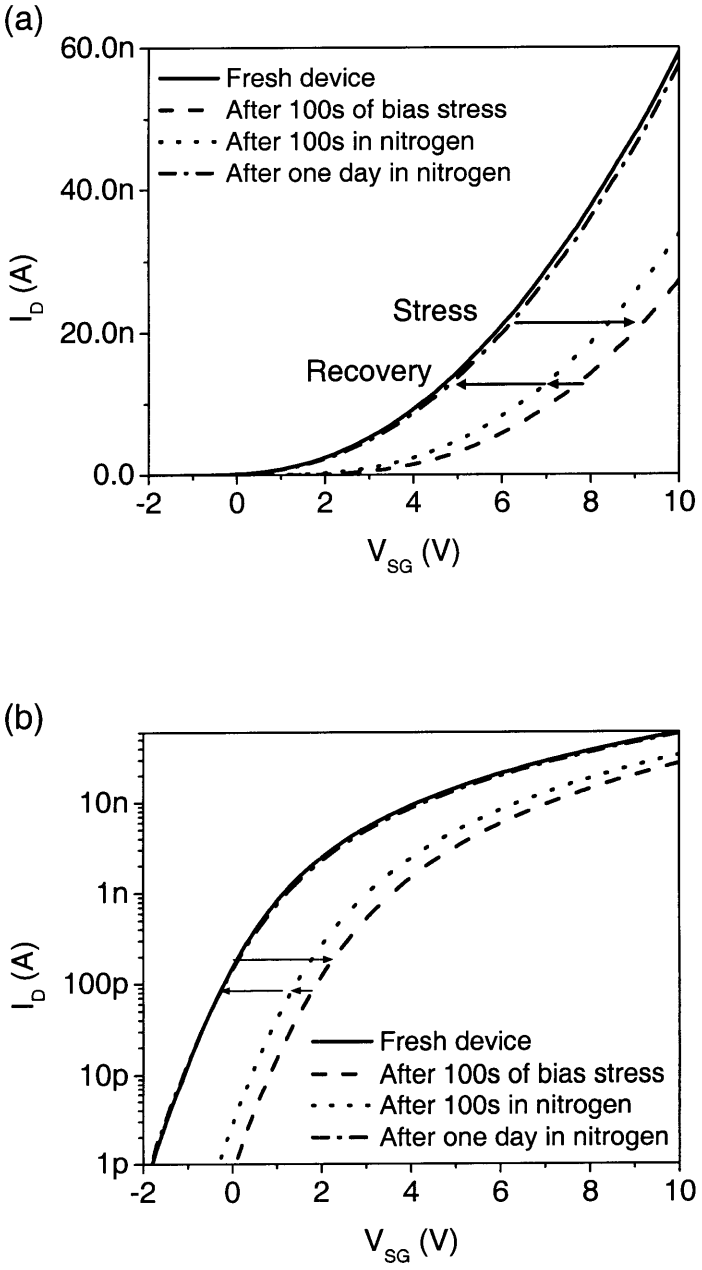

Figure 6-1: Transfer I-V characteristics before stress, after stress, and after 100s, and 1 day in nitrogen in the dark with all the electrodes grounded. The bias stress condition was V_{SG} = 30 V, V_{SD} = 1 V for 100 s. The measurement is taken on a 1000/25 μm transistor in nitrogen ambient. (top) Linear and (bottom) semilog plots show that the recovered I-V characteristics are identical to the original I-V characteristics.

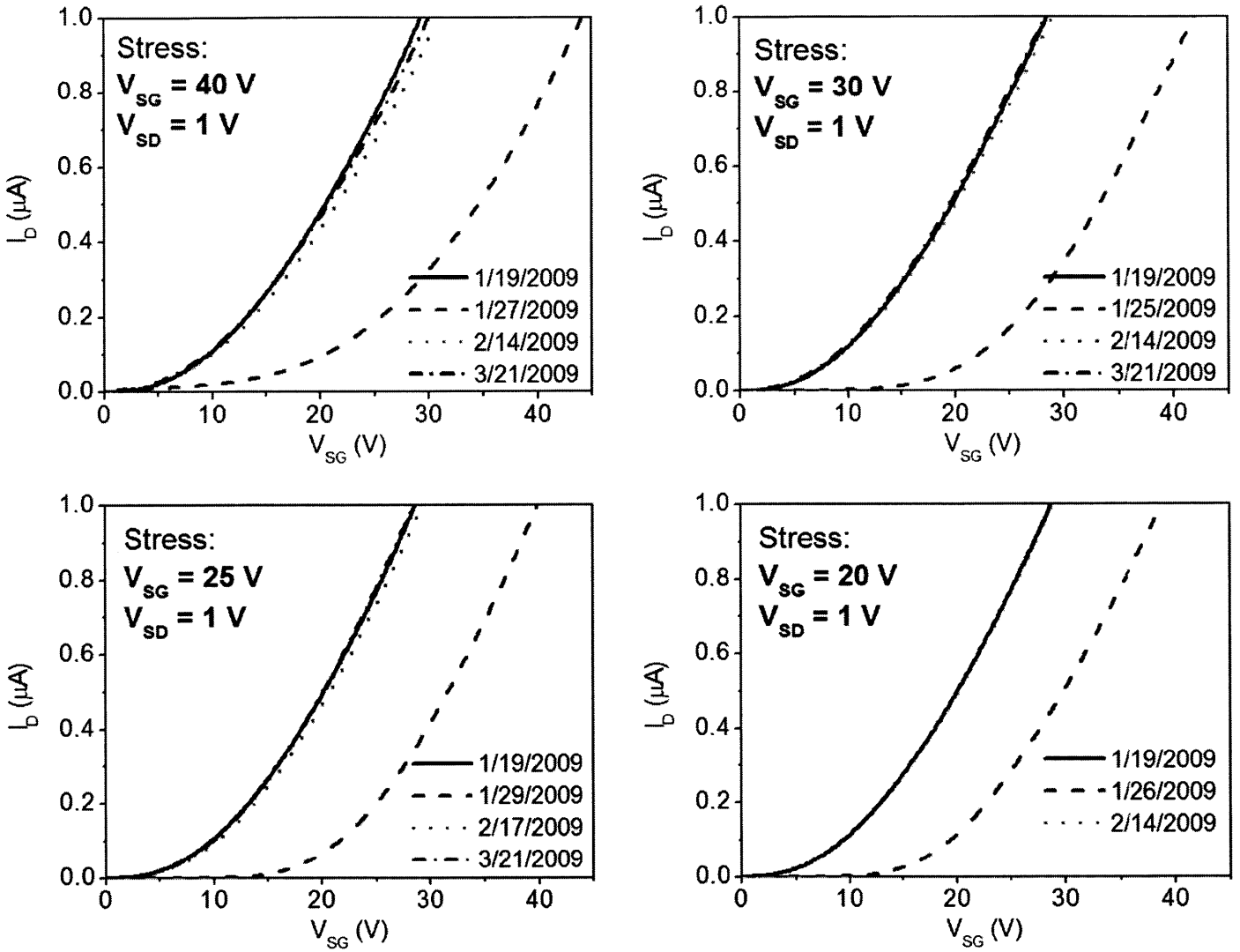

Figure 6-2: Transfer I-V characteristics before (solid line) and after the stress (dashed line), and after the recovery (dash-dot line). Complete recovery is observed for different stress conditions. The applied stress conditions are shown in the inset. The dates the measurements were taken are noted to give a sense of the recovery time. Devices were in nitrogen ambient with no bias applied during recovery.

6.1 I-V Recovery Characterization

The lack of current during the recovery makes it impossible to do on-the-fly measurements to study the recovery. Hence precise time dependence is difficult to measure. Moreover, the recovery measurements have inherently more measurement error than the stress measurements because the devices must be stressed before a recovery can be measured. Errors introduced during the stressing phase add to the total measurement error. Here the recovery is studied by grounding the electrodes and taking intermittent I-V sweeps, after the application of the stress condition. Although it is difficult to quantify and model the recovery precisely, the qualitative dependencies of recovery to time, temperature, and gate voltage are identified. All the measurements were taken in nitrogen ambient in the dark at 20 ^{o}C unless noted otherwise.

6.1.1 Recovery Time Dependence

The recovery time dependence was measured by first stressing a device at V_{SG} = 30 V, V_{SD} = 1 V until the ΔV saturated and measuring ΔV during the recovery phase for a hundred thousand seconds. The recovery of the device was performed by grounding all the terminals. The recovery was interrupted initially every minute to take the measurements to quantify the ΔV. The interval between the measurements was increased to ten minutes as the recovery progressed. The resulting measurement is shown in Figure 6-3.

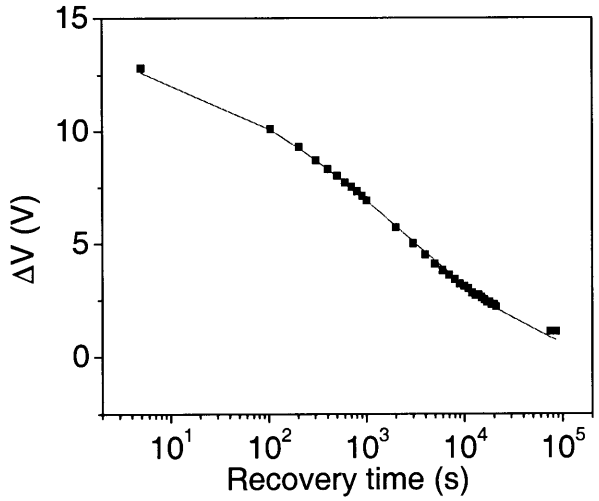

Figure 6-3: Time dependence measurement of recovery of stressed devices. The solid line is the fit to a stretched-exponential equation.

The time dependence of the recovery is found to be well modeled by the stretched-exponential equation similar to the BSE. The link between the BSE and its recovery is strengthened by the study of the BSE on two wafers with different BSE time constants. The different time constants originate from an annealing process on one of the wafers which makes it more robust against the BSE. Devices on both wafers are stressed until they have ΔV of 5 V at 40 °C at V_{SG} = 35 V, V_{SD} = 1 V. For the unannealed device, this ΔV is reached in 100 seconds, while for the annealed device it takes 500 seconds. After the same ΔV is achieved for both devices, the ΔV is measured during the recovery. Figure 6-4 shows that the recovery on the annealed device, which has slower BSE, is also slower. Through this observation, the detrapping time constants are found to be closely related to the trapping time constants.

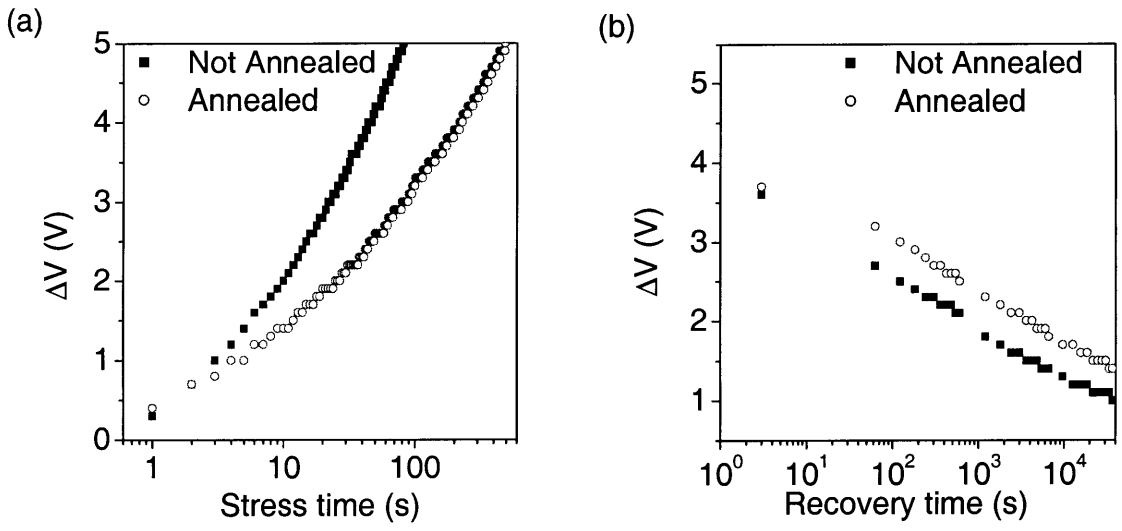

Figure 6-4: Comparison of stress measurements (a) and recovery measurements (b) in devices on different wafers. Devices on annealed wafer have both slower BSE and recovery. Both devices are stressed to $\Delta V = 5$ V, and recovered at 40 °C.

6.1.2 Temperature dependence

To identify the activation energy for the recovery, the temperature dependence was measured. First the initial I-V characteristics were taken at different temperatures to quantify ΔV in the recovery phase. The transistors were then stressed at 20 °C for 1000 seconds. The stress induced an equal ΔV of 6.7 V in all the measured transistors. After the stress phase, the transistors entered the recovery phase by grounding all the terminals. At the start of the recovery phase, the temperature was changed to the desired temperature for recovery. Figure 6-5 shows that there is a clear trend of faster recovery for higher temperatures.

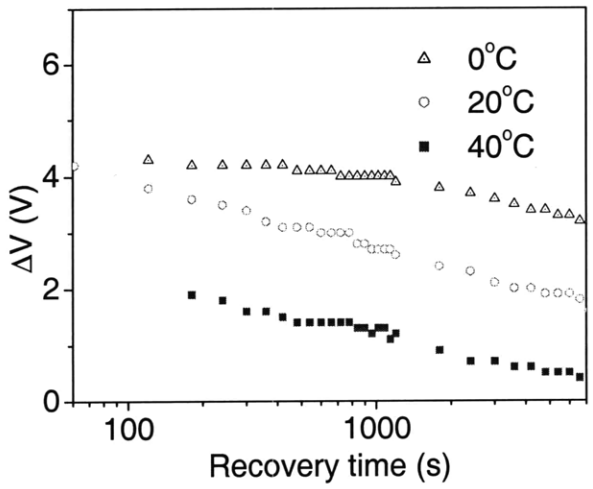

Figure 6-5: Temperature vs. recovery after equal stress of V_{SG} = 35 V, V_{SD} = 1 V for 1000 s at 20 °C. ΔV = 6.7 V at t = 0 s for all three transistors.

Although the measurement in Figure 6-5 shows qualitative recovery trend for different temperatures, the measurement is inadequate for quantitative analysis as there is a temperature transition region where the temperature is changed from 20 °C to the temperature of interest at the start of the recovery phase. Depending on the temperature, it can take up to a minute for the temperature to settle to a steady value. To quantify the effect of temperature on the recovery, both stress and recovery have to be performed at the temperature of interest. Because the speed of the BSE is different for different temperatures, the stress time has to be controlled to achieve the same amount of ΔV. The stress time is controlled by monitoring the ΔV with on-the-fly measurement. After the devices are stressed for ΔV of 5 V, the recovery is monitored from 0 to 40 °C. The measured data is then fit to a stretched-exponential equation to extract τ and β. The extracted activation energy from the resulting τ is 0.8 eV. The activation energy is the same as the one measured for the stress, which also indicates that the recovery mechanism is closely tied to the stress mechanism.

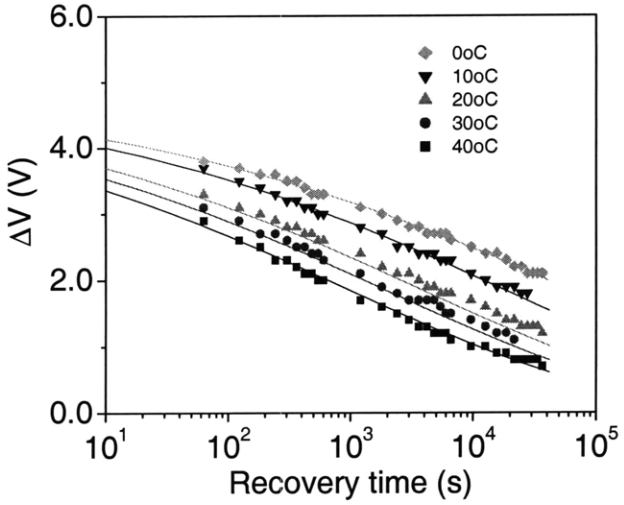

Figure 6-6: ΔV vs. recovery time at the respective temperatures. The transistors are first stressed until ΔV = 5 V. The dots represent the data and the lines represent the fit to the stretched-exponential equations.

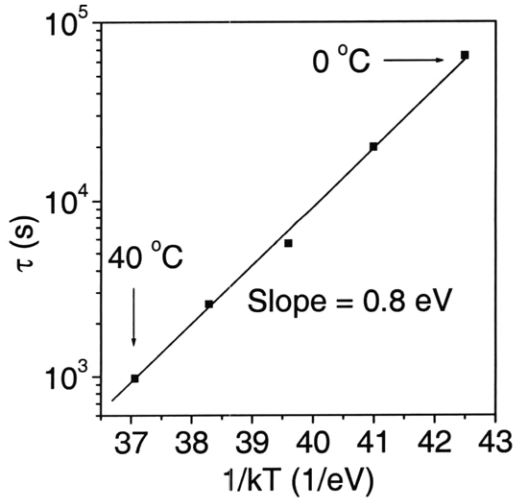

Figure 6-7: Arrhenius plot of τ vs. 1/kT for the extraction of activation energy for τ.

6.1.3 V_{SG} Dependence

The effect of V_{SG} on recovery is measured next. After a transistor is stressed, the recovery is monitored by grounding the source drain terminal and biasing the gate of the transistor at different values. It is found that large values of negative V_{SG} noticeably accelerate recovery.

The negative V_{SG} does not induce any carriers in the channel as the pentacene channel does not invert and no electrons are injected through the gold electrodes. Therefore we conclude that the electric field alone accelerates the recovery. The field may lower the barrier that a trapped carrier must hop out of and thus accelerate the recovery.

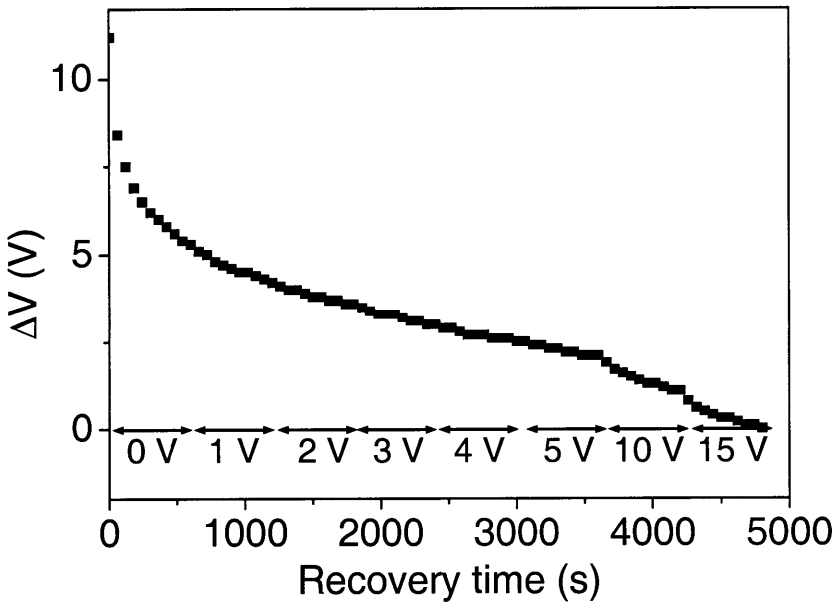

Figure 6-8: Recovery as a function of time. Every 600 seconds the gate voltage during the recovery phase is stepped up starting from 0 V to 15 V. It is found that stepping up the V_{SG} from -5 V to -10 V and from -10 V to -15 V significantly increase the recovery rate. Measurements were taken at 40 °C.

6.2 Charge Recovery Measurement

Since the recovery is due to the detrapping of the carriers in the channel, the recovery rate can be measured directly from the current due to the detrapped carriers. However this recovery current is small. A quick calculation shows that if the recovery rate is about 1 V/100 s, the current is Q/t = Ci × 1 V × Area/ 100 s. For a 1000/5 μm device with Ci = 15 nF/cm^2, this current is about 7.5 fA. Because the current scales with the total channel area, a device with a large area must be used. A transistor with 2000 μm width and 150 μm length would yield 60x current and is used for the measurement. In addition, the current is integrated to measure the charge, which makes the measurement more robust.

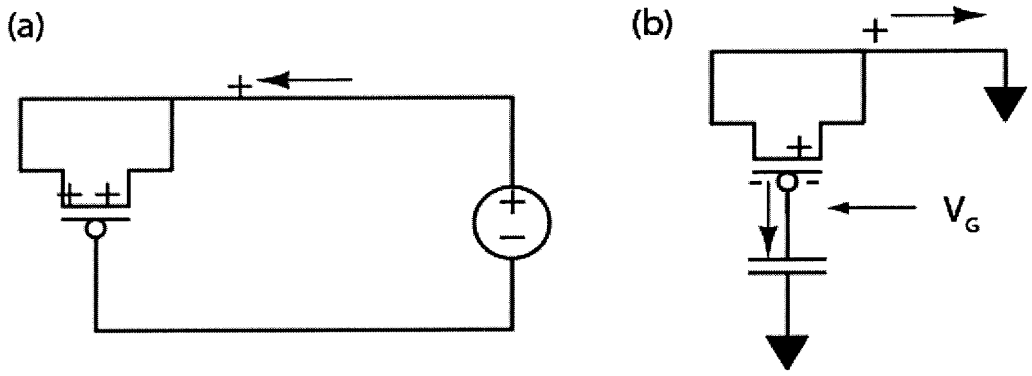

Figure 6-9: Direct measurement of the recovery rate by measuring charge due to detrapped carriers. Measurement set up during stress (left) and during recovery (right). Recovery is measured by monitoring the voltage at the gate.

To measure the charge of the detrapped carriers during recovery, the transistor is first stressed. In this phase, the mobile carriers are slowly trapped. In the recovery phase, the bias stress is removed and grounded for a brief period to let all the mobile carriers escape the channel. Then the source/drain electrodes are grounded to let the carriers detrap, and the gate is connected to a small capacitor. As the charge detraps, the corresponding negative charge fills the capacitor, and the voltage change can be read accordingly as illustrated.

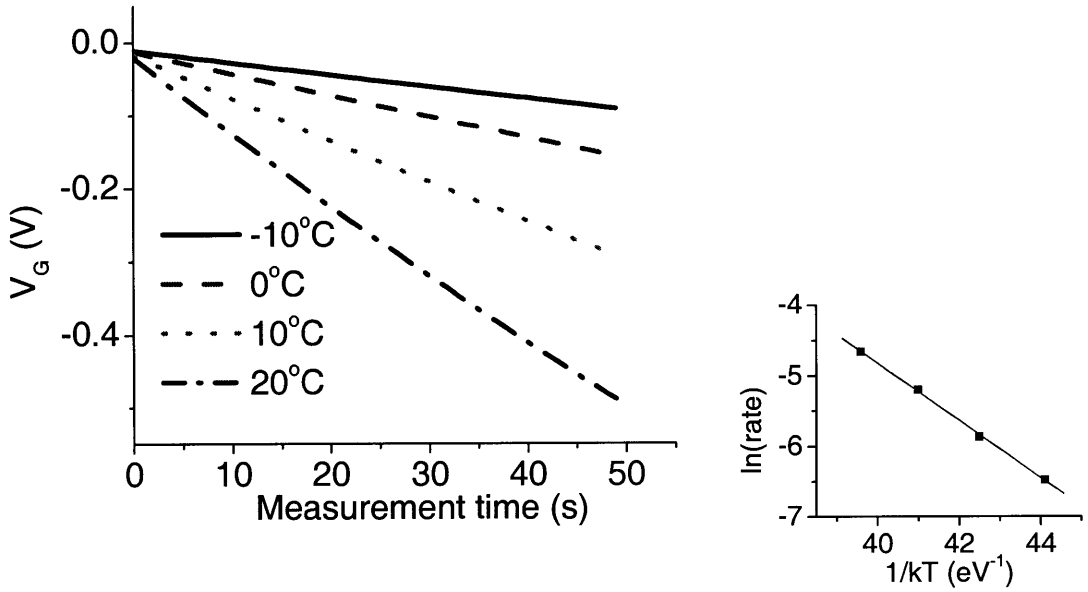

Figure 6-10: Charge measurement for different temperatures. A stress of 300 seconds at V_{SG} = 30 V, V_{SD} = 1 V is applied to the device before the charge measurement. The detrapping charge in the channel induces a drop in the gate voltage. The rate is slowed as the temperature decreases.

The charge measurement verifies the temperature dependence of the recovery rate. The temperature change induces change in the speed that the capacitor is charged. From this change, the activation energy of the detrapping rate can be measured from an Arrhenius plot as shown. The activation energy of the detrapping rate is 0.72 eV; which is close to the extracted activation energy of τ in the previous section.

Next, a similar charge measurement is performed on a metal-insulator-metal (MIM) capacitor. The MIM capacitor is integrated on the same wafer as the transistors and uses the same parylene gate dielectric. If the trapping is occurring in the bulk of the parylene, a similar response will result from the charge measurement in a MIM capacitor. However, MIM

capacitors show no charge detrapping after a stress is applied to it. Therefore we conclude that the presence of the pentacene is required for the traps to exist. The location of traps is at the parylene and pentacene interface because this is where the carriers are accumulated, based on the QSCV measurements.

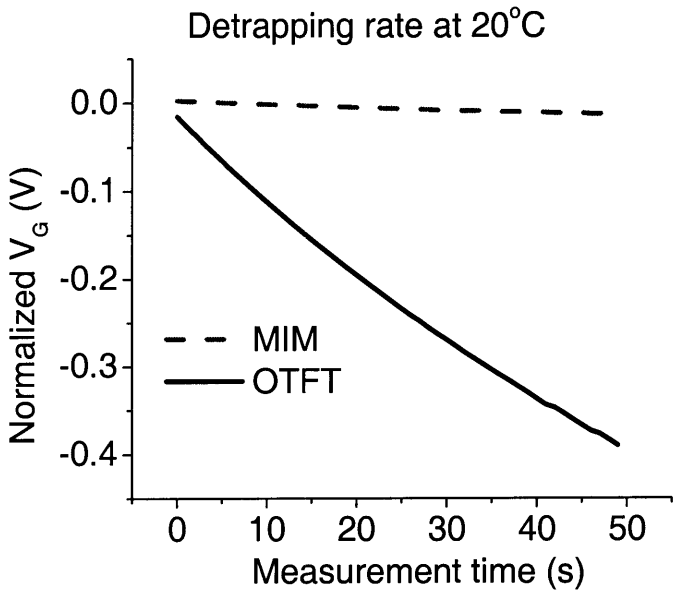

Figure 6-11: Charge measurement from a MIM capacitor and an OTFT. The voltage change due to detrapping of the trapped carriers during recovery phase is measured. The voltage is normalized by the area of each device. The MIM capacitor shows no significant change in the voltage compared to the OTFT indicating that the traps are located at the parylene/pentacene interface.

6.3 Mechanisms

In a-Si:H TFTs, trap creation has been noted as the main cause of the BSE. We show that traps are not created in pentacene OTFTs by showing that stressing does not change the number of trap states in the OTFTs. This is done by first stressing the device to achieve saturation of the ΔV. The number of trap states is inferred from ΔV_{FINAL}. The OTFT is then recovered and stressed again for the second time. If the stress creates states which cause the BSE, the trapping rate will be faster and ΔV_{FINAL} will be higher for the second stress phase. It is found that the trapping rate for the second stress is no faster than the first, and that the same ΔV_{FINAL} is achieved as shown in Figure 6-13. Therefore it is unlikely that the BSE in OTFTs is caused by trap creation.

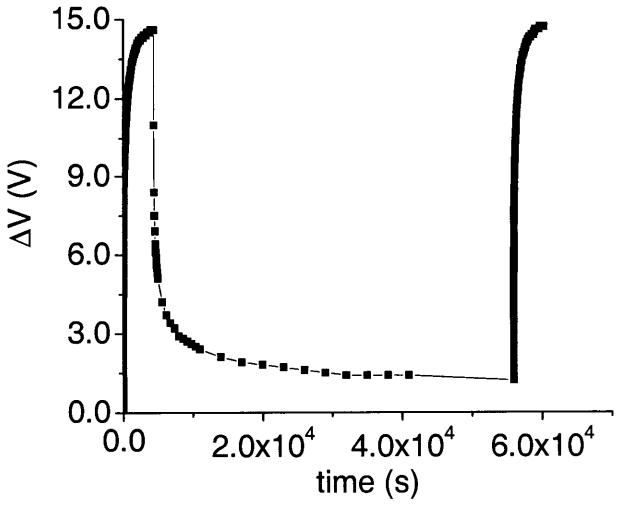

Figure 6-12: Stress-recovery-stress measurement. The ΔV is plotted throughout the measurement. The OTFT is first stressed for 5000 s at V_{SG} = 35 V, V_{SD} = 1V, and recovered for a 50000 s and stressed at identical stress conditions for a second time. At 40 °C.

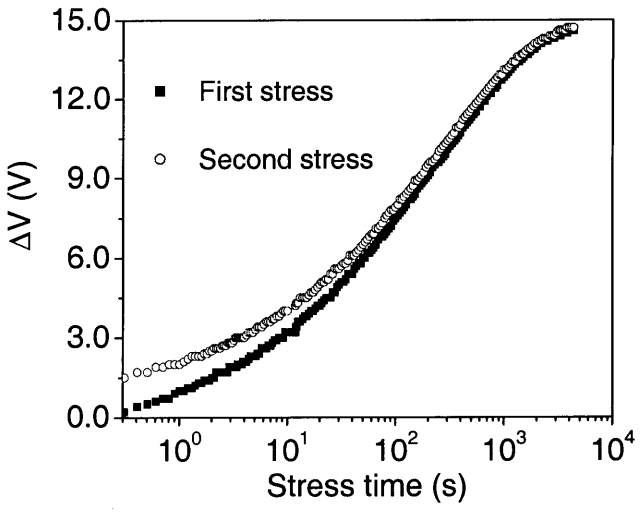

Figure 6-13: Repeated stress measurements. ΔV data from Figure 6-12 are replotted with respect to the stress time. The second stress measurement has some residual ΔV left from the previous stress measurement. It can be noted that the trapping rate has not increased and the BSE saturates at the same ΔV. All measurements were taken at 40 °C.

In polymer TFTs, bipolaron formation has been proposed for the cause of the slow channel carrier trapping [4]. The bipolarons are pairing of two holes, which are energetically favorable in polymers. Such pairing of two holes is hindered by Coulomb repulsion and is responsible for the barrier to trap. For bipolarons the trapping rate is proportional to the square of the hole concentration because two holes are needed to form a bipolaron. However, in the measured transistors the trapping rate is proportional to the cubed of the hole concentration, indicating that another mechanism is responsible for the BSE.

Previously, Gu et al. have proposed that the detrapping of electrons trapped in the semiconductor causes the BSE in pentacene OTFTs [5]. This mechanism explains the observed BSE by detrapping of electrons which are initially trapped in the semiconductor gap states. The application of a negative bias on the gate electrode (positive V_{SG}) repels

electrons trapped in the channel and detraps them. This results in the decreased drain current due to the decrease in the extra holes that balanced the trapped electrons. Although such a mechanism explains the long time constant associated with the BSE, a fast recovery of the original I-V characteristics would be expected when the stress is removed. However, it has been observed that time constants related to recovery are comparable to the BSE.

We propose that the mechanism for the BSE is the trapping of channel carriers in states located at the semiconductor/dielectric interface over a barrier. When the channel is populated by the holes, the holes do not trap in the defect states immediately as they must first hop over a barrier for them to be trapped. During the recovery, the trapped carriers must again hop over a barrier in order to detrap. The barrier to access each defect state is disordered in nature which causes the dispersion of time constants and results in the stretched-exponential time dependence. The barrier is lowered for high fields, which accounts for the fact that faster trapping and detrapping occurs with higher fields. The existence of the barrier also explains the observed temperature dependence of both the BSE and its recovery.

The defect states can either be at the parylene side of the interface or the pentacene side of the interface. The sources of defect states in the parylene can be dangling bonds formed by detached H^+ ions. These dangling bonds would serve as trap states for the holes. The physical separation between the pi orbitals in the pentacene where the holes are induced and the defect states in the parylene is the source of the barrier. The separation is on the order of a few Å as the C-H bond at the edge of both the pentacene and the parylene is on the order of 1 Å.

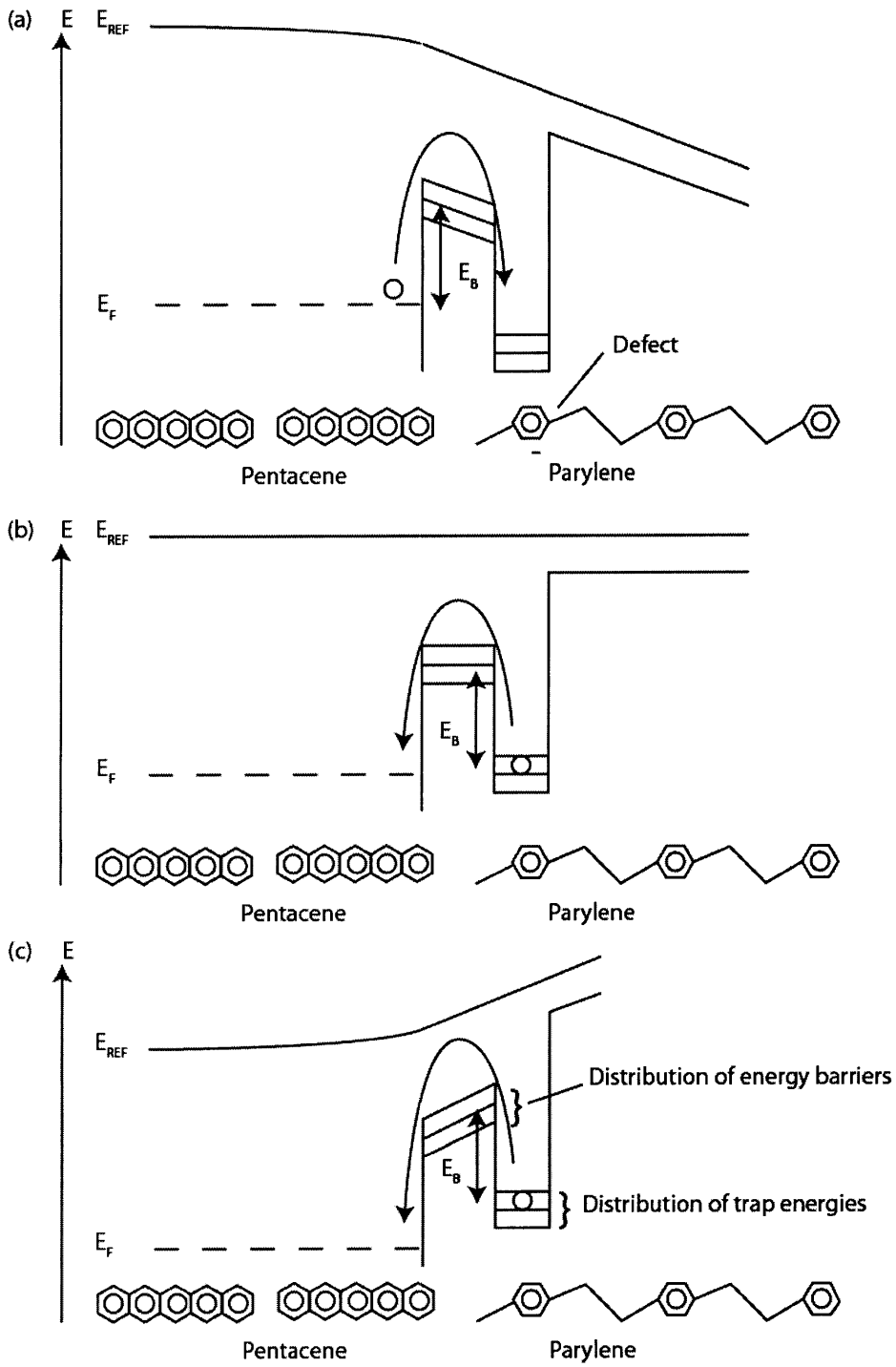

Figure 6-14: Band diagram for (a) $V_{SG} > 0$, (b) $V_{SG} = 0$, and (c) $V_{SG} < 0$. The energy levels for holes are drawn, with a reference energy with respect to the vacuum level. Trapping is shown in (a), and detrapping is shown in (b) and (c). The trapping occurs by channel carriers hopping over a barrier to access the defect states. The recovery occurs by release of the trapped carrier over a barrier in the reverse direction. The Fermi energy in the channel is modulated by the V_{SG} and dictates whether trapping or recovery occurs. The V_{SG} also accelerates trapping and detrapping via barrier lowering.

Another possible source of traps may be the pentacene itself. Due to the disorder in the pentacene, it may have deep trap states which are spatially and energetically isolated. These states can take a long time to access and brought to equilibrium so that the traps are filled according to the Fermi energy set by the channel [6]. Holes occupying and emptying these traps can account for the observed BSE and its recovery.

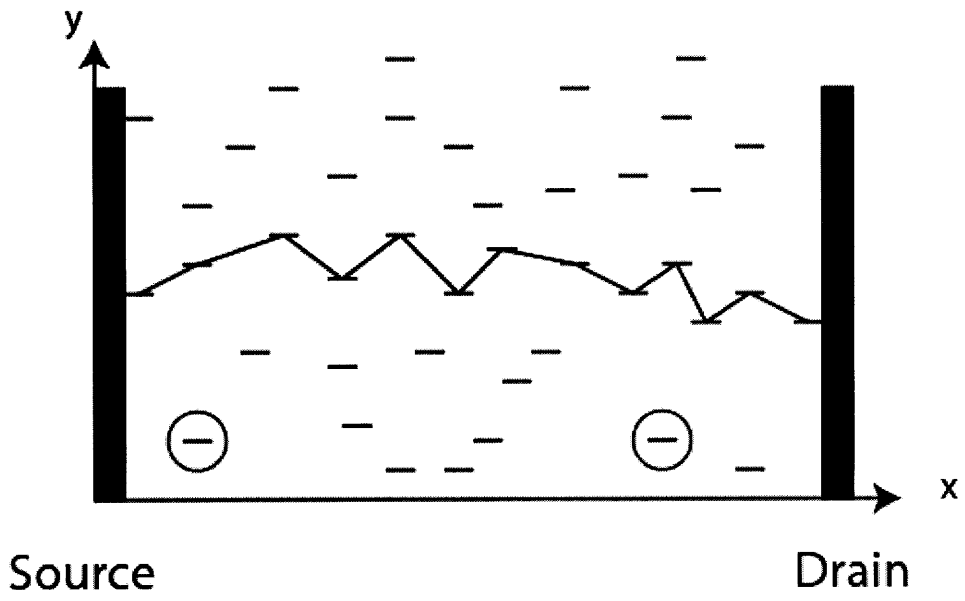

Figure 6-15: Representation of traps spatially distributed through the channel. The conduction is mainly due to the states which are spatially and energetically close to one another (connected lines in the middle). The states are shown only in the spatial domain for illustrative purposes. Due to the disorder, there are states that may be spatially and energetically isolated from the nearest neighbors (circled states). These spatially isolated states can take long for carrier population to equilibrate to the Fermi level and can act as trap states that cause the BSE.

6.4 **Summary**

In this chapter, the recovery of the BSE was studied in detail. We find that the recovery is closely linked to the BSE as it has similar stretched-exponential dependence on time and thermal activation energy. In addition, the recovery on annealed devices, which have slower BSE, is also slower supporting that the sources of long time constants for the BSE and its recovery are the same. The experimental observations indicate that the recovery is through detrapping of carriers hopping over the same disordered barriers as in trapping. Applying negative V_{SG} and supplying field across the channel accelerates the recovery. By employing the recovery charge measurement technique, which measures the recovery directly from the charge due to the detrapped carriers, we found that traps are not located in the bulk of the parylene.

Physical mechanisms which may be responsible for the BSE were discussed next. To first exclude the possibility of trap creation causing the BSE, stress-recovery-stress measurements were performed. We found no change in the number of trap states caused by stressing. Thus we conclude that trap creation is not responsible for the BSE. We propose that trapping and detrapping of channel carriers in states which have barriers to access is responsible for the BSE and its recovery. The mechanism can be described by trap states that are difficult to access and must be accessed by carriers occupying an energetically unfavorable energy state. Some possible sources of the trap states and barriers were mentioned.

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Chapter 7

Annealing to Reduce the Bias-stress Effect

In this chapter we explore annealing processes to reduce the BSE. It has been previously reported that annealing a completed device at 140 °C in nitrogen ambient for eleven hours suppressed the BSE in top-contact pentacene OTFTs [1]. This post-process anneal (PPA) is found to increase contact resistance in the bottom-contact OTFTs studied in this work. Therefore a new annealing process is developed. The new annealing process reduces the BSE so that it takes over eight times longer to induce the same amount of ΔV and improves the electrical characteristics by increasing the mobility and reducing the contact resistance. The annealed devices are studied in detail to explain the source of the reduced BSE.

7.1 Annealing Process

First, an annealing process on completed devices (PPA) is explored. The completed devices are annealed in nitrogen at different temperatures and measured again at 20 °C. I-V sweeps are measured on identical devices to analyze the effect of annealing. It is found that above 60 °C I-V characteristics begin to change as shown in Figure 7-1.

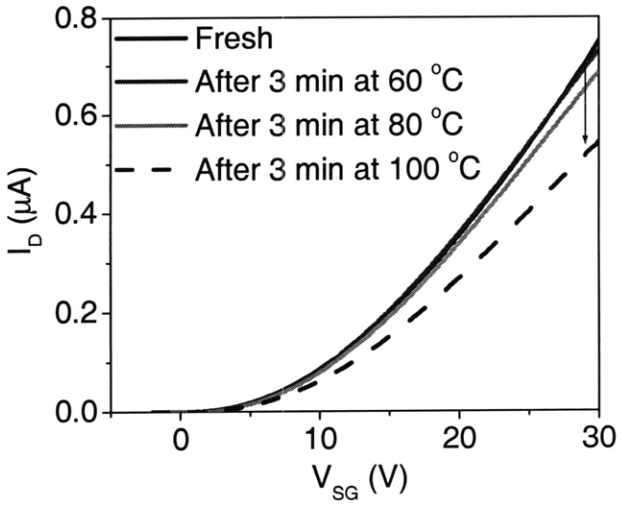

Figure 7-1: Linear I-V characteristics change due to post-process anneal at different temperatures. Measurements were done on a 1000/5 μm device with V_{SD} = 1 V.

The shape of the I-V characteristics changes indicating that the degradation is not caused by gate voltage shifts. After annealing at 120 °C in nitrogen for ten minutes, the current degrades from 4.4 μA to 2.5 μA for a 1000/5 μm device at $V_{SG} = V_{SD}$ = 20 V. To identify the cause of the current degradation, the extracted device parameters are compared before and after the PPA. It is found that the current is degraded neither by mobility degradation nor a threshold voltage shift, but due to the increase in the contact resistance. The contact resistance increase may be explained by morphological changes in the contact region. It has been reported that the morphology of pentacene grown on top of electron-rich gold is different from that grown on top of a gate dielectric [2]. The different pentacene morphologies lead to stressed regions at the intersection of these two films that lead to high contact resistances. As the films expand and contract during the annealing process, the morphology of this highly stressed region can change and increase the contact resistance. Top-contact devices do not suffer from such effects because the pentacene is grown on top of the gate dielectric regardless of contact or channel regions and have no phase boundaries.

This observation explains why an increase in contact resistance has not been reported after annealing of top-contact transistors. The PPA is regarded to be unsuitable for reducing the BSE for bottom-contact transistors because of the degradation of the I-V characteristics.

To avoid the increase in contact resistance, a new annealing process is developed. Because it is postulated that the contact resistance increase occurs because of the morphological changes in the pentacene, the new annealing process involves annealing the device after the patterning of the S/D electrodes and before the deposition of pentacene. Annealing condition is 120 °C

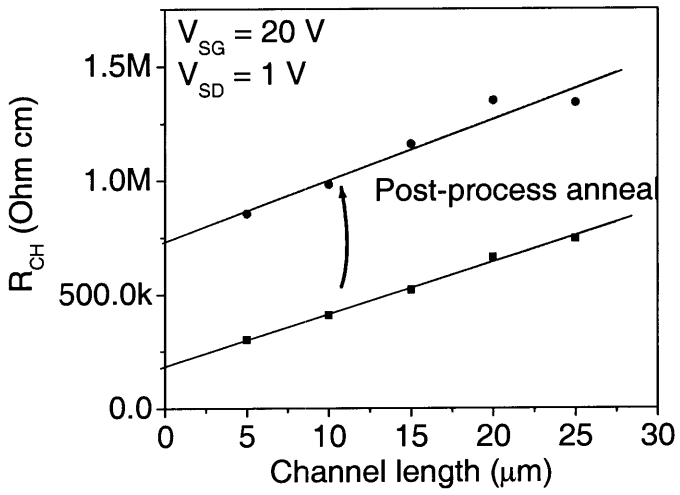

Figure 7-2: Contact resistance extraction before and after the PPA. The slope of the line, which is inversely proportional to mobility, has not changed indicating that the mobility has not changed while the y-intercept, which is the contact resistance, has increased by four folds. PPA condition was 120 °C in nitrogen for ten minutes.

	Before Anneal	After PPA	
R_c	185	736	KΩ-cm
Mobility	0.014	0.014	cm^2/Vs

Table 7-1: Parameter comparison before and after the PPA. The extracted parameters show that the degradation is caused by the increase in the contact resistance. Measurements were taken on the same devices.

in a nitrogen backfilled oven for ten minutes. It is found that the new process of annealing prior to deposition of pentacene (APDP) increases the mobility and significantly lowers the contact resistance compared to the control. The anneal process also reduces the BSE as shown in Figure 7-5.

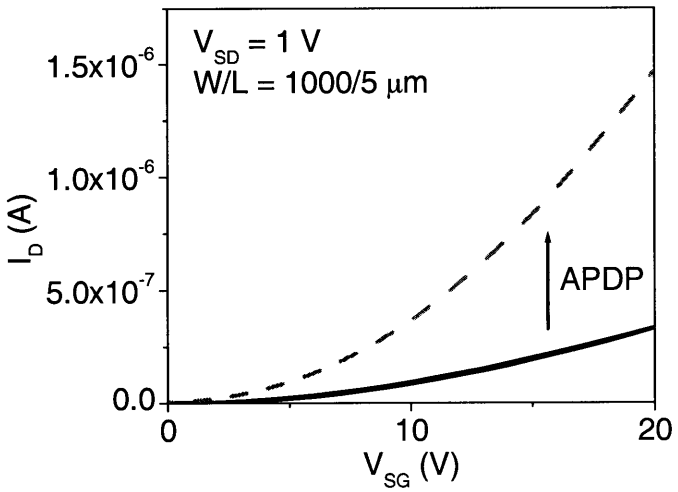

Figure 7-3: I-V characteristics with and without the APDP process.

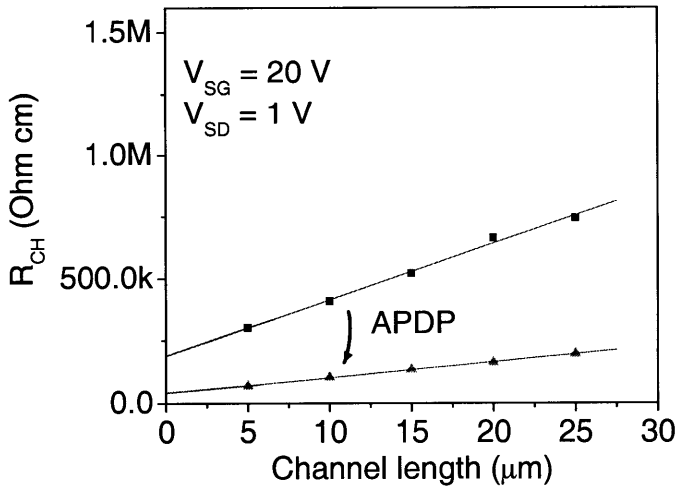

Figure 7-4: The contact resistance extraction of devices with and without the APDP process. The slope of the line, which is inversely proportional to mobility, is reduced indicating an increase in mobility. APDP condition is 120 °C in nitrogen for ten minutes.

	Control	APDP	
R_c	185	38	KΩ-cm
Mobility	0.03	0.05	cm^2/Vs

Table 7-2: Parameter comparison of devices with and without APDP. The APDP devices have less contact resistance and higher mobility.

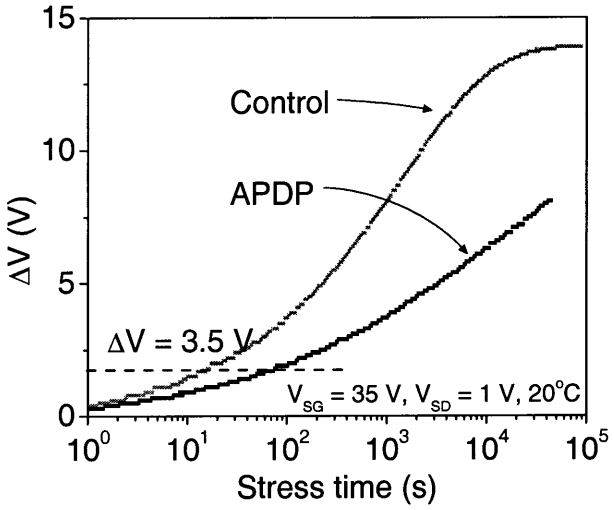

Figure 7-5: The BSE on devices with and without APDP. The APDP devices have less ΔV after the same bias-stress conditions.

One way to measure the reduced BSE is the time it takes to induce the same amount of ΔV. This time is directly connected with the circuit lifetime and reliability. Using the circuit lifetime criteria introduced in Chapter 5, the circuits fabricated out of APDP transistors will have eight times improved lifetime when the circuit fails at $\Delta V/V_{DD}$ = 10%, or ΔV = 3.5 V. For higher ΔV, the lifetime on APDP devices will be greater than eight times of control devices as seen by the diverging graph in Figure 7-5.

To identify what has led to the improved electrical characteristics, tapping mode AFM was taken on parylene with and without the annealing process. Because smoothness of the dielectric layer has been closely related to the mobility of pentacene OTFTs [3], it was

expected that the annealed parylene film would be smoother. However, the rms roughness on the annealed parylene (1.8 nm) has been found to be slightly higher than that on the unannealed parylene (1.6 nm) indicating surface roughness is not responsible for the better mobility. However, there is significant change in the phase image of the AFM indicating that the surface energy is different. The higher contrast on the annealed parylene indicates that there is less interaction between the silicon tip and the parylene surface. This in turn indicates lower surface energy on the annealed parylene.

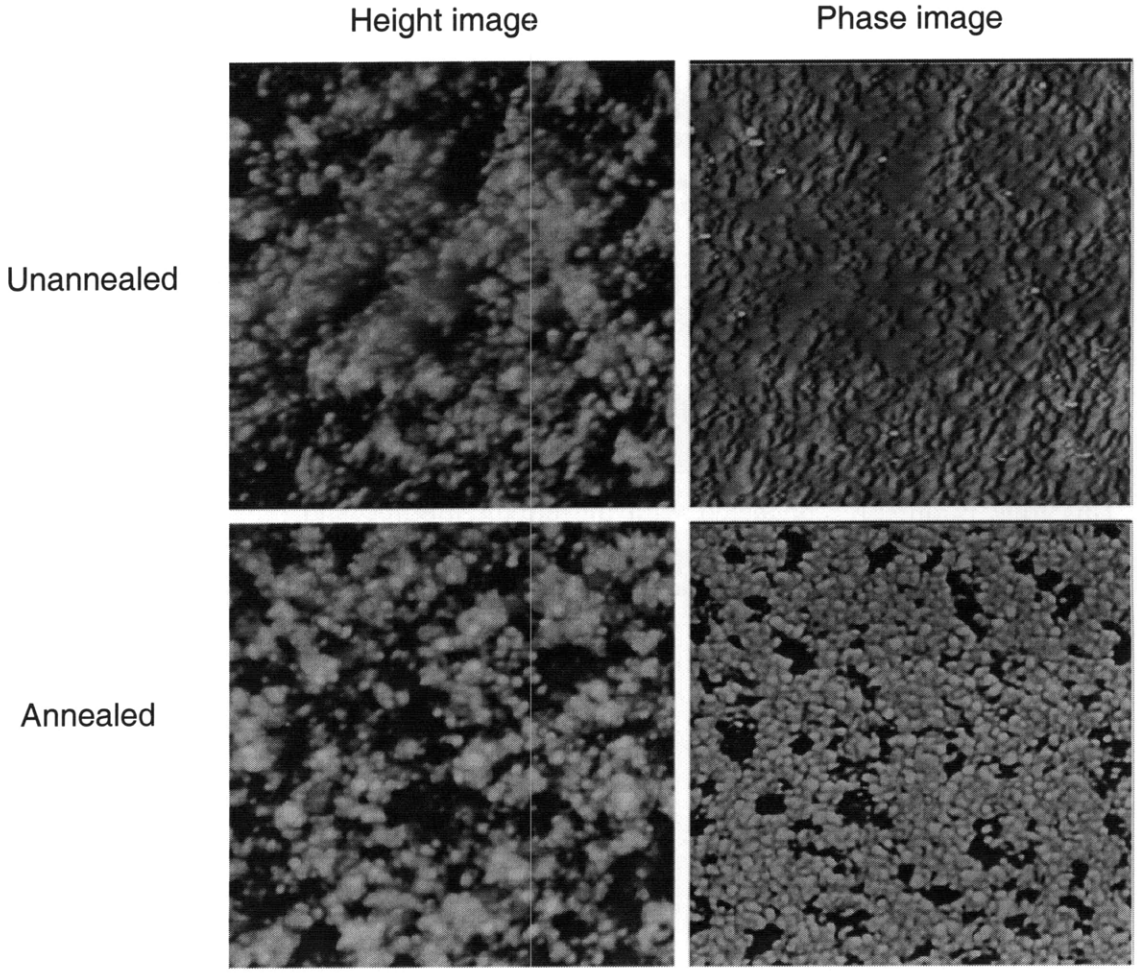

Figure 7-6: AFM on unannealed and annealed parylene. Height image is shown in the left and phase image is shown in the right column. There is no discernable difference in height image, but the phase image is different indicating that the surface energy is different. The scan area is 1 μm x 1 μm. Height range = 10 nm, phase range = 50°.

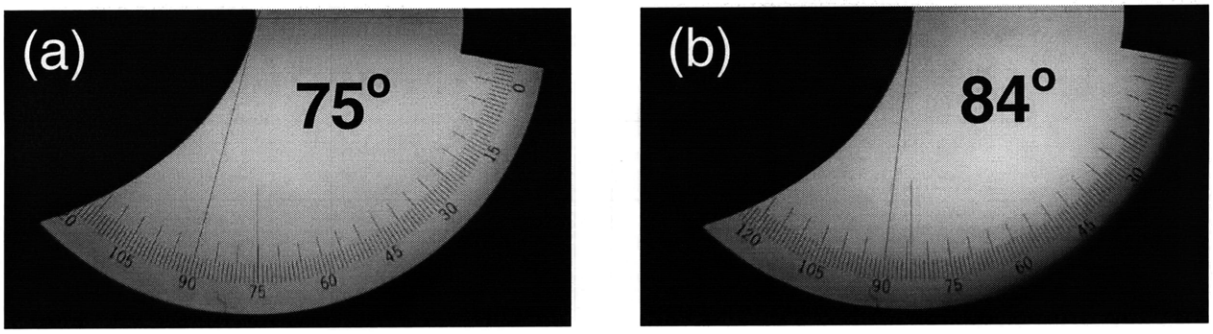

Figure 7-7: Water contact angle measurements on parylene. (a) before annealing (b) after annealing. After annealing, parylene has higher contact angle indicating a lower surface energy.

To assert the lower surface energy on the annealed parylene, DI water contact angles are measured on both parylene surfaces. Consistent with the measurements from the AFM, the water contact angle on annealed parylene shows lower surface energy indicated by higher water contact angle [4]. It has been reported previously that lower surface energy leads to higher mobility in pentacene OTFTs [5]. The improved electronic characteristics results from the improved microstructures at the interface which may also be the source of improved stability.

Different annealing times are explored to optimize the annealing time. Table 7-3 summarizes the results from different annealing times. It is found that among the measured annealing times, 45 min annealing time yielded the best result at 120 ^{o}C. At very long annealing times, it is found that the contact resistance increases.

	Control	APDP annealed		
Annealing time (min) [1]	0	10	45	1000
mobility (cm^2/Vs) [2]	0.030 ± 0.004	0.050 ± 0.003	0.050 ± 0.001	0.06 ± 0.02
$R_{CONTACT}$ (KΩ-cm) [2]	185 ± 0.9	38 ± 0.3	38 ± 0.1	75 ± 0.8
ΔV (V) [3]	7.6 ± 0.1	2.6 ± 0.04	1.8 ± 0.06	2.9 ± 0.6

[1] All annealing were taken place at 120 °C

[2] Taken at V_{SG} = 20 V

[3] ΔV after 300 s of stress at V_{SD} = 30 V, V_{SD} = 0.1 V

TABLE 7-3: RESULTS FROM DIFFERENT ANNEALING TIMES.

7.2 Measurements of the Bias-stress Effect on Annealed Devices

The BSE in the APDP transistors is investigated in detail to determine the source of the reduced BSE. First, a long stress test is done at 40 °C to determine if the density of traps (N_T) in the channel has decreased. Figure 7-8 shows that the ΔV_{FINAL} is measured to be 12 V on the APDP transistors which is lower than 14 V of the control devices, indicating that the density of traps is less for the APDP transistors. The ΔV_{FINAL} can be directly compared between the APDP devices and control devices tested in Chapter 5 because the parylene dielectric was deposited at the same time, and hence C_i is the same for both devices.

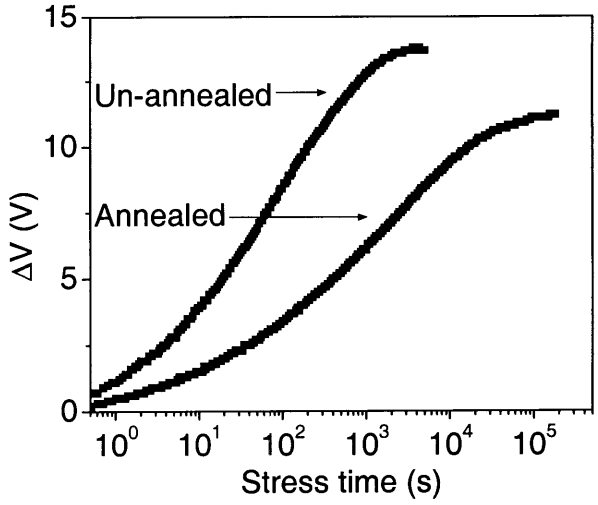

Figure 7-8: Extended time stress measurements for annealed transistors at 40 °C. Stress condition is V_{SG} = 35 V, V_{SD} = 1 V.

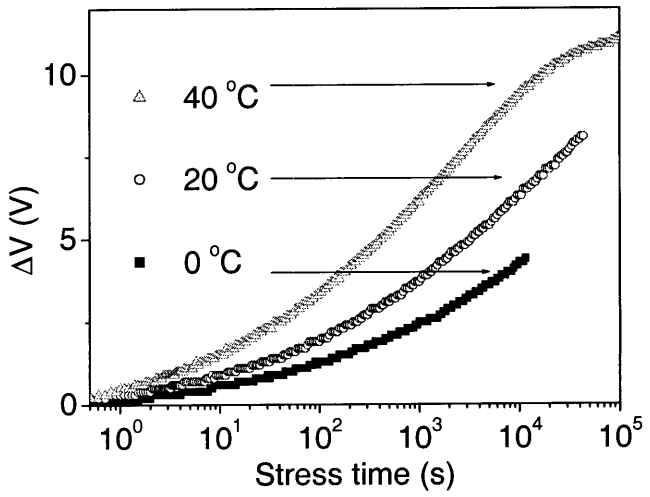

Figure 7-9: Temperature dependence of bias-stress in annealed transistors. Stress condition is V_{SG} = 35 V, V_{SD} = 1 V.

Stress T (°C)	Stress V_{SD}(V)	Stress V_{SG}(V)	ΔV_{FINAL} (V)	τ (s)	β
40	1	35	12	2900	0.35
20	1	35	12	23000	0.33
0	1	35	12	131000	0.30

Table 7-4: Fitting parameters for data shown in Figure 7-9.

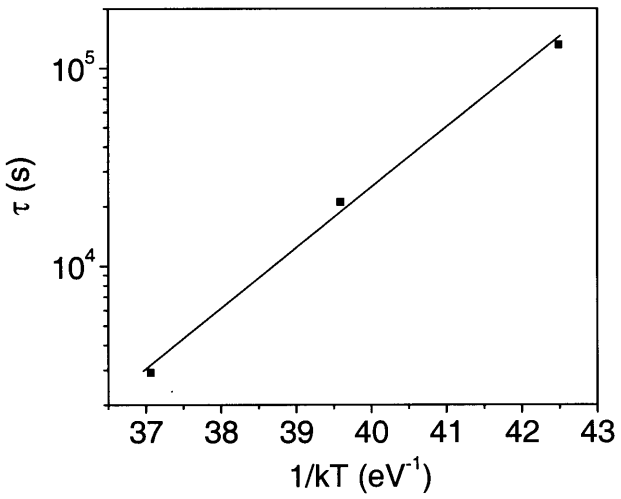

Figure 7-10: Activation energy for data in Table 7-4. The activation energy for APDP transistors is 0.7 eV.

It is observed that the reduced BSE also results from an increase in τ. For example at 40 °C the τ increases from 140 seconds on control devices to 2900 seconds on the APDP devices as shown in Table 7-4. To see if the increased τ is due to the increased energy barrier for the carriers to be trapped, the temperature dependence of the BSE is measured. The BSE measurements are taken on three different temperatures at 0, 20, 40 °C at V_{SG} = 35 V, V_{SD} = 1 V, same as the measurement conditions for extracting the energy barrier for the control devices. Arrhenius plot of the τ in Figure 7-10 shows that the activation energy for τ in APDP devices is 0.7 ± 0.04 eV which is lower than the activation energy for τ in controlled devices at 0.8 ± 0.04 eV. The lower activation energy of τ in the annealed devices comes as a surprise as it would lead to shorter trapping time constants and result in faster BSE. However, the comparison of the activation energy of τ in the control devices and the annealed devices is not straightforward because the density of the total traps has decreased as observed in the decrease in ΔV_{FINAL}, and the dispersion of energy barriers has increased as

observed from the decrease in β. A more careful study of the DOS vs. E_B needs to be considered to make any valid claims if annealing changes the energy barriers and further understand the cause of the increased τ due to annealing.

7.3 **Summary**

An annealing process to improve the stability as well as the mobility and the contact resistance has been developed. Process involved annealing the devices just prior to the deposition of pentacene at 120 ^{o}C in a nitrogen backfilled oven. The annealing lowered the contact resistance by 4x and improved the mobility as well. The annealed devices had less trap states indicated by the lower ΔV_{FINAL} and also had slower trapping rate indicated by a larger τ. The temperature measurements show that the larger τ is not due to the increased energy barrier but due to the temperature independent factors. The temperature independent factors in the time constants may be explained by the increase in the average hopping distance in the annealed devices.

[1] T. Sekitani, S. Iba, Y. Kato, T. Someya, and T. Sakurai. Suppression of DC bias stress-induced degradation of organic field-effect transistors using postannealing effects. *Appl. Phys. Lett.*, 87:073505, 2005.

[2] I. Kymissis, C. Dimitrakopoulos, and S. Purushothaman. High-performance bottom electrode organic thin-film transistors. *IEEE Trans. Electron Devices,* 48:1060-1064, 2001.

[3] S.E. Fritz, T.W. Kelley, and C.D. Frisbie. Effect of dielectric roughness on performance of pentacene TFTs and restoration of performance with a polymeric smoothing layer. *J. Phys. Chem. B*, 109(21):10574-10577, 2005.

[4] J. Yu. *Improving OLED Technology for Displays.* PhD Thesis, MIT, Cambridge, 2009.

[5] S.Y. Yang, K. Shin, and C.E. Park. The effect of gate-dielectric surface energy on pentacene morphology and organic field-effect transistor characteristics. *Adv. Funct. Mater.*, 15:1806-1814, 2005.

Chapter 8

Conclusions and Future Work

8.1 **Conclusions**

OTFTs are promising for flexible large-area electronics. Owing to the organic semiconductors' low thermal requirements, they can be deposited on any substrate at room temperature. This allows them to be fabricated on plastics and even on paper. In addition, the organic semiconductors can be deposited with low-cost, mass production techniques such as roll-to-roll printing processes or inkjet printing. However, the bias-stress effect in OTFTs causes operational instability which prevents OTFT technology from being used in a range of circuit applications. This work presents a systematic study of the BSE in integrated OTFTs using pentacene semiconductor and introduces an annealing method to reduce the BSE.

It is found that the BSE results from carriers that are trapped in the semiconductor/dielectric interface. The BSE can be accurately modeled by a shift in the gate voltage, ΔV, which equals qN/C_i. where N is the density of the trapped carriers, and C_i is the capacitance of the channel normalized by area. It is shown that both gate field and channel carriers are needed

to cause the BSE, and drain current does not cause the BSE. Because the trap density is limited, when there are more carriers induced in the channel than available number of traps, ΔV saturates at a constant value, ΔV_{FINAL}, proportional to the trap density in the channel. This behavior of ΔV saturating despite there being free carriers in the channel is observed for the first time in any TFT. The implications of fixed density of traps have been modeled to correctly predict stress behaviors at low V_{SG}.

It is found that the time constants associated with the traps are dispersed due to the disorder in the material, and the ΔV results in a stretched-exponential stress time dependence. Fundamental understanding of the stretched-exponential parameters τ and β is gained by theoretically modeling the trapping process. This model explains the various parameter dependencies in the temperature stress data. From the temperature measurements, the long time constants for trapping are found to be due to a high energy barrier for carriers to be trapped.

The dependency of the BSE to various bias-stress conditions is identified and expressed in an equation, which allows for the prediction of ΔV for different stress times and voltages. The equation estimates the implication of the BSE on circuit applications and usable lifetime. We find that the V_{DD} should be under the operation point where $p = N_T$ for optimum circuit lifetime. We observe that full recovery of the BSE occur when bias-stress is removed in pentacene OTFTs. The recovery has been found to have time dependency and thermal activation energy that is same as the BSE. Moreover the recovery time is found to be proportional to the BSE time indicating that the source of long time constants for both the

BSE and its recovery is of the same origin. A trapping model that accounts for the BSE and the recovery is presented.

A new annealing process which improves mobility and reduces contact resistance and the BSE has been developed. The annealed OTFTs have mobility of 0.05 cm^2/Vs and contact resistance of 38 KΩ-cm compared to 0.03 cm^2/Vs and 185 KΩ-cm in the control devices. The BSE is reduced by the reduction of the density of trap states and by the increase in τ by over ten fold. The increase in τ has been found to be due to the increase in non-temperature dependent factors.

8.2 **Future Work**

There are interesting works in both the scientific and the engineering domain to further our understanding of the BSE and to increase the OTFT stability. This work provided a framework for systematically characterizing the BSE in TFTs. Most importantly, it developed a method to extract the density of traps in the interface and model trapping time constants. The framework to characterize the BSE can be extended to other OTFTs with different structures and semiconductors. Moreover it can also be used for TFTs that use inorganic semiconductors.

Further experiments can be designed to understand the origin of the traps as it would be beneficial for both scientific and engineering reasons. The traps can be caused by structural defects inherent in the pentacene semiconductor or in the parylene dielectric. Identifying the

physical source of defects would lead to better understanding of the BSE and methods to further improve stability. For example, to identify if exposure to chemicals such as the gold etchant is causing the defects, lift-off patterning of the S/D layer can be employed. To identify whether defects in pentacene or defects in parylene are responsible for causing the BSE, an approach used by Podzorov et al. can be employed [1]. In such an approach, the semiconductor film can be grown on the same surface, and flipped on to a structure with prefabricated gate and source drain contacts with different gate dielectrics. Growing the pentacene films on the same surface will ensure the same morphology of the pentacene films and allow true isolation of effects due to different gate dielectrics. In contrast, if pentacene films are grown on different dielectrics, morphological changes will result depending on the surface energy and surface roughness [2,3], which will obscure the effects due to change in the dielectric and change in the pentacene morphology.

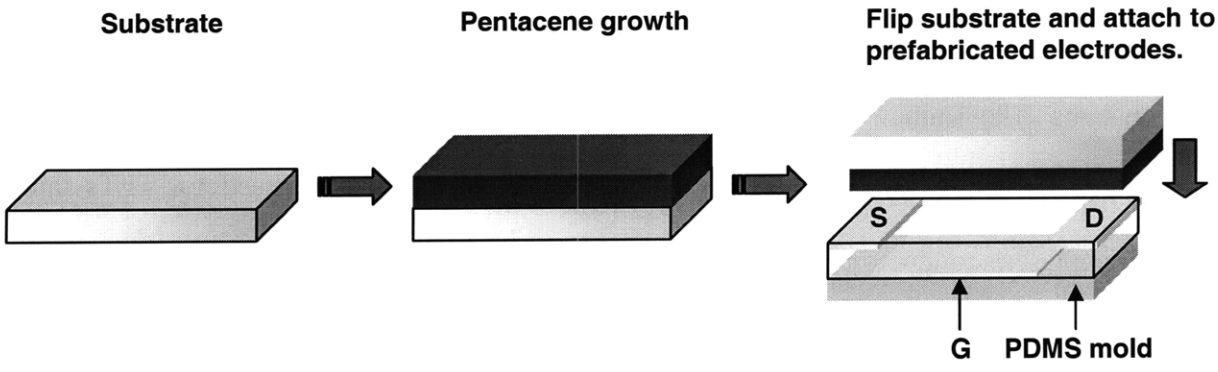

Figure 8-1: Fabrication of OTFTs using separate growth of organic semiconductor thin films. In such an approach, the effect of the semiconductor film morphology and the dielectric can be separated.

In addition, further optimization of the annealing process can be explored to increase stability. For example, different anneal temperatures and ramp/cool rates can be explored to increase the stability in the integrated pentacene OTFTs. The engineering of the annealing process should be accompanied by the study of the changes in the physical properties of the parylene surface with the use of surface characterization techniques such as AFMs and Auger Spectroscopy. The change in the morphology of the pentacene film on annealed parylene should also be studied in detail with the use of AFM at different pentacene deposition thickness.

Better encapsulation should be developed so that the devices can be stored in air without degradation. Figure 8-2 shows an example hybrid parylene/metallic encapsulation which can be employed on the integrated OTFTs used in this work. The encapsulation would only add a metal deposition step after the deposition of the parylene encapsulation layer and would not incur additional patterning step. The use of hybrid parylene/metallic encapsulation has shown to increase device lifetime in air significantly in other pentacene OTFTs [4].

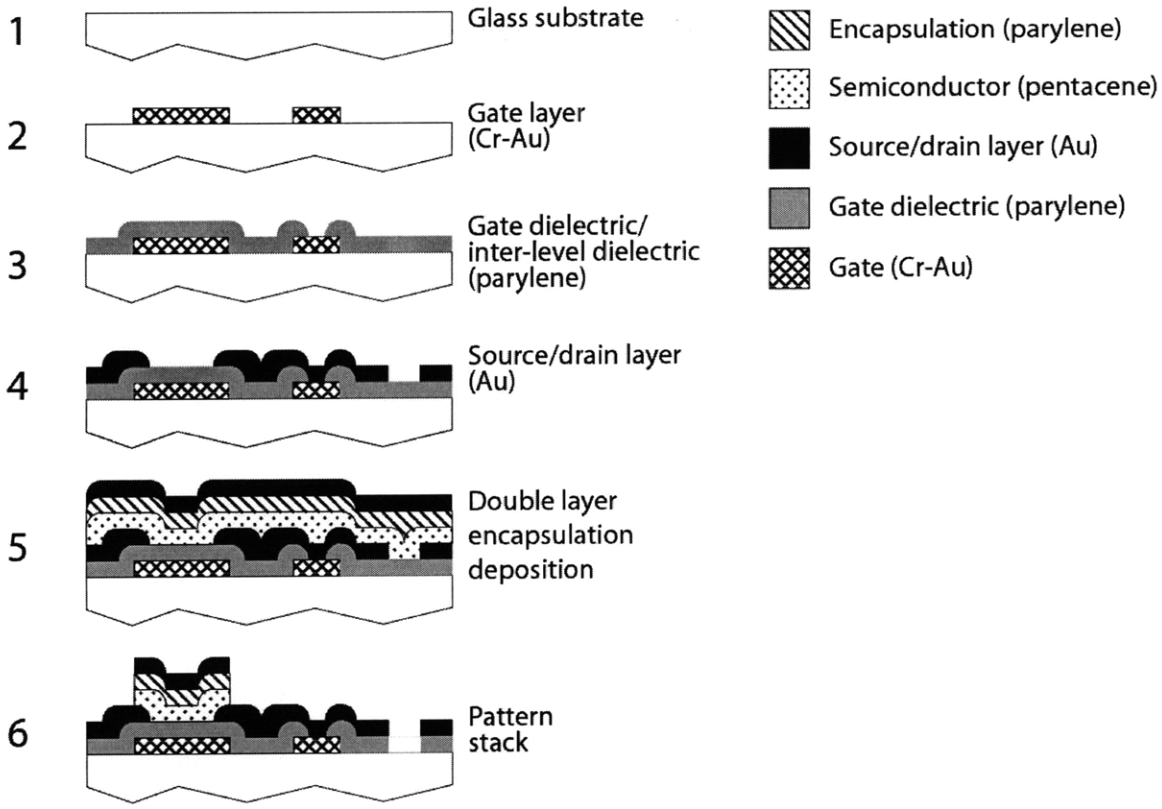

Figure 8-2: Integrated process of OTFTs with hybrid organic/metallic encapsulation.

[1] V. Podzorov, E. Menard, A. Borissov, V. Kiryukhin, J.A. Rogers, and M.E. Gershenson. Intrinsic Charge Transport on the Surface of Organic Semiconductors. *Phys. Rev. Lett.*, 93:086602, 2004.

[2] S.E. Fritz, T.W. Kelley, and C.D. Frisbie. Effect of dielectric roughness on performance of pentacene TFTs and restoration of performance with a polymeric smoothing layer. *J. Phys. Chem. B*, 109(21):10574-10577, 2005.

[3] S.Y. Yang, K. Shin, and C.E. Park. The effect of gate-dielectric surface energy on pentacene morphology and organic field-effect transistor characteristics. *Adv. Funct. Mater.*, 15:1806-1814, 2005

[4] T. Sekitani and T. Someya. Air-stable operation of organic field-effect transistors on plastic films using organic/metallic hybrid passivation layers. *Jpn. J. Appl. Phys.*, 46:4300-4306, 2007.

Appendix A Process Flow for MIT OTFTs

All process was done in the Technology Research Laboratory located within building 39 at the Microsystems Technology Laboratories.

	Process	Machine	Parameters
#	**CLEAN SUBSTRATE**		
1	Piranha clean	acidhood	Standard Piranha clean. Mix 1:3 = H_2O_2:H_2SO_4 and immerse wafers in solution vertically for 10 minutes. Follow by DI water rinse and SRD.
	GATE		
2	Deposit Cr/Au	ebeamAu	Deposit 100 Å of Chrome followed by 600 Å of Au at 2 Å/s.
3	Photolith Pattern Mask - G	EV1	Spin coat OCG825, std recipe: 500/750/3000 rpm 6/6/30 s. Prebake resist for 25 min at 95 oC in an oven. Expose for 1.6 s. Develop in OCG934 until clear (90 s). SRD.
4	Etch Au (time)	acidhood	Mix 5:1 = DI water:Au etchant. Etch for 80 seconds while moving the wafers horizontally.
5	Etch Cr (time)	acidhood	Mix 1:1 = DI water:Cr etchant. Etch one wafer at a time until clear (15~25 s). SRD.
6	Strip resist	photo-wet-Au	Sonicate at power 3 in Microstrip for 10 min. Rinse in DI water. Soak in bubbler for 1 minute. SRD
7	Observe under Microscope		Check if all the test patterns have come out.
	GATE DIELECTRIC		
8	Deposit gate dielectric	parylene	Weigh 1 g of parylene N. (200 nm). Set parylene machine to 670 °C pyrolysis/165 °C evaporation/25 mtorr. Lay wafers flat in the chamber. Zero thickness monitor and press start.
	VIA		
9	Photolith Pattern Mask-VIA	EV1	Spin coat AZ5214 std condition. Prebake at 95 °C for 30 min. Expose 1.6 s AZ5214, 90 s dev
10	Etch Via	plasmaquest	parylene.rcp for 180 s.
11	Strip Resist	photo-wet-Au	Same as step 6.
	SOURCE DRAIN		
12	Deposit Au	ebeamAu	400 Å at 2 Å /s .
13	Photolith Pattern Mask-S/D	EV1	Same as step 3. 2 s exposure.
14	Etch Au (time)	acidhood	Same as step 4. Etch for 60 s.
15	Strip Resist	photo-wet-Au	Same as step 6.
	SEMICONDUCTOR		
16	Deposit semiconductor	pentacene	195 °C 20 min
17	Deposit Encapsulation	parylene	Same as step 8.
18	Photolith Pattern Mask-ACT	EV1	Same as step 3.
19	Etch active layer	plasmaquest	parylene.rcp for 180 s.

DI: De-ionized, SRD: Spin rinse dry.

Appendix B Parameter Extraction of OTFTs

1. Overview

There is a growing interest in low-temperature thin-film transistors as they are attractive for making large-area applications such as displays and sensors that are flexible or built on durable plastic substrates. However, it is difficult to compare the performance of lab-developed transistors because they vary in so many different ways. This short article is written to outline some of the parameters that should be measured as a method of transistor bench-marking. The symbols used in this document follow the definitions in IEEE Standard 1420. As an example of applying the outlined characterization method, several samples of pentacene field effect transistors (FETs) were characterized.

In designing circuit applications with the new thin-film transistors, we can go in one of two ways: we can determine the operation voltage and then characterize the transistors with those constraints in mind, or we can design the system after we have characterized the transistors. In this document we will use the former method. A supply voltage of 20 V, which is used widely by the display industry, was assumed for the characterization of the transistors.

This document is written with pFETs in mind as pentacene FETs are pFETs. When applying the illustrated characterization method on nFETs, the polarity of the voltage is reversed. To avoid confusion, when a voltage is "decreased" it is in the direction where it will induce less channel current.

2. Measurements

Although there are many parameters that need to be considered, a few quick measurements can tell a lot about the transistor performance. There are three key measurements that will be used to extract parameters. All the following measurements should be done in double sweeps to observe the effect of hysteresis.

2.1 Output characteristics

With V_{SD} as var1, and V_{SG} as var2, V_{SD} is varied from 0 to 20 V with V_{SG} taking three to four steps from when it is off to when it is fully on. From these measurements, we can observe the effects of the injection barrier, and verify that the device is truly a transistor. See Figure 1.

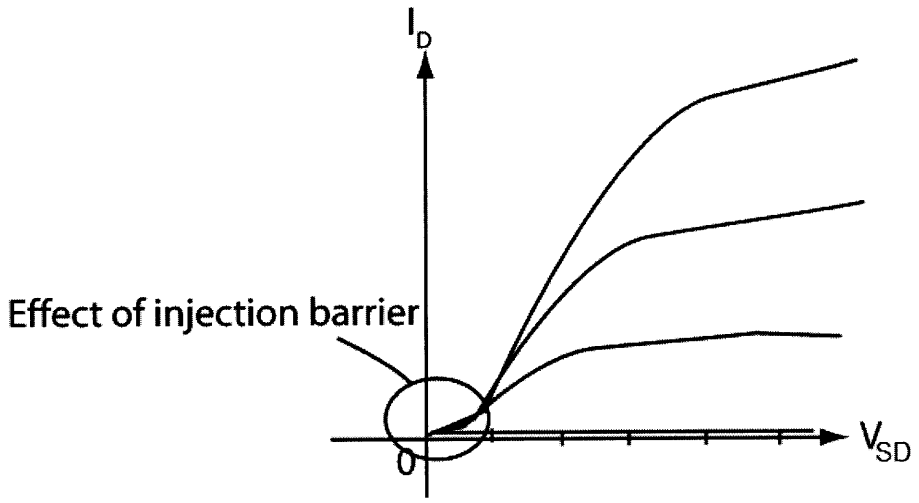

Figure B-1. Output Characteristics. The non-ideal beak-like shape at low V_{SD} is due to the injection barrier.

2.2 Linear region transfer characteristics
With V_{SG} as var1, and V_{SD} as var2, V_{SG} is varied from -20 to 20 V (off to on) with V_{SD} at 1 V. With this measurement, gate leakage, subthreshold slope, mobility and contact resistance can be extracted.

2.3 Saturation region transfer characteristics
With V_{SG} as var1, and V_{SD} as var2, V_{SG} is varied from -20 to 20 V with V_{SD} at 20 V. With this measurement, channel leakage, subthreshold slope, threshold voltage, on/off ratio, and I_{ON} can be measured.

2.4 C-V measurement
Because of the high contact resistance, capacitance should be measured using the QSCV measurement technique or low frequency (<100 Hz) C-V measurement. Agilent 4156C was used to make the measurements. With V_{SG} as var1, source and drain connected and grounded, the V_{SG} is varied from -20 to 20 V. The ramp rate is 83.33 mV/sec, hold time is 1 sec, delay time is 0, step size is 100mV. Parasitic capacitance and the channel capacitance can be measured, and the threshold voltage measured in the transfer characteristics can be verified.

3. Measured Parameters

3.1 Gate leakage current ($I_{G,leak}$)
Leakage current is crucial when measuring how long the transistor can hold a charge. It will determine the V_{OFF}, the gate voltage as when the channel leakage current drops below gate leakage current. Because there will be no benefit of applying a lower gate voltage, V_{OFF} is the lowest voltage we will be applying to the gate in switching applications. $I_{G,leak}$ = gate current at V_{SG} = 20V when we are measuring CV measurements using quasi-static technique. We can also measure leakage current by measuring I_G with V_{SG} = 20 V and V_{SD} = 0 V after a

long hold time. Leakage current can be reduced by increasing the dielectric thickness, the quality of the dielectric, and reducing the overlap between source/drain and the gate layer.

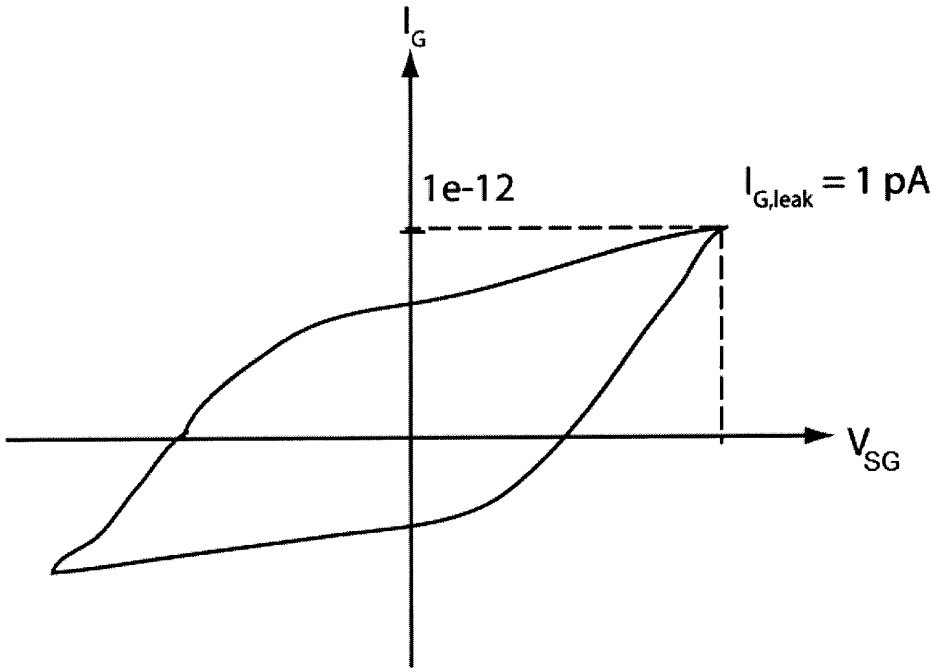

Figure B-2. Gate leakage current from linear region transfer characteristics.

3.2 Channel leakage current ($I_{SD,leak}$)
Channel leakage current makes up for the other component of the leakage current and is important for the same reasons gate leakage current is important. Usually in OTFTs the channel leakage current is lower than the gate leakage current as the mobility in these transistors can be quite low. The existence of high channel leakage current indicates parasitic pathways of leakage currents.

3.3 Subthreshold slope (S)
This slope determines what the voltage swing should be given an on/off ratio, and determines what the refresh rate should be when the voltage swing is set. The subthreshold slope also decides the power dissipation of the circuit because power =½CV_{DD}^2 per switching. It is the inverse of the slope of the linearly exponential part in a semilog plot of the transfer characteristics outlined in Section 2.3. The units are V/dec.

3.4 On/off ratio
This determines how long the capacitor can hold the charge when it is switched with this transistor. Given the voltage swing of 20 V, we measure this by having V_{SD} = 20 V, and V_{SG} – V_{OFF} = 20V.

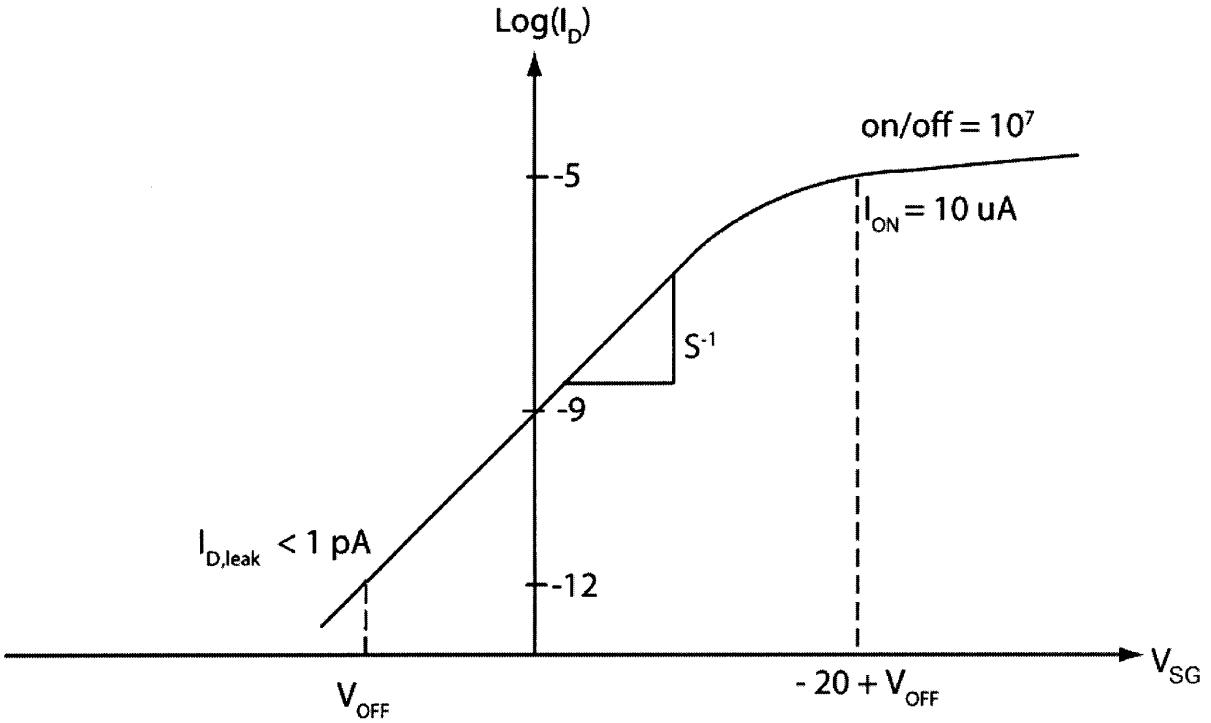

Figure B-3. Saturation region transfer characteristics. $I_{SD,leak}$, V_{OFF}, S, I_{ON}, on/off ratio can be determined.

3.5 I_{ON}

This lumps together mobility, channel length, and the contact resistance. It determines how fast we can drive the circuits ($\tau \sim CV_{DD}/I_{ON}$), or how much current it can supply to an OLED, etc. It is the current measured at a V_{SD} = 20 V, $V_{SG} - V_{OFF}$ = 20 V. Because current scales proportionately with width, the device width needed for a certain current output can be determined with this knowledge.

3.6 Parasitic Capacitance (C_P)

This also determines circuit speed. It is the capacitance deep in the depletion (positive V_{SG}). This should be minimized when speed is wanted, but can be used as a charge storage element when it can be controlled accurately.

3.7 Channel Capacitance (C_{Ch})

This also determines how much charge injection there will be. It is the capacitance of the transistor in accumulation minus the parasitic capacitance. This is approximately equal to WLC_{OX}.

3.8 Hysteresis (V_{SHIFT})

In order to make precise and fast circuit applications hysteresis should be minimized. It can be minimized by reducing the interface state density between the gate dielectric and the semiconductor. It can be quantified by how much the C-V curve shifts in voltage. When comparing hysteresis, the C-V measurement should be done at the same speed, hold time, etc.

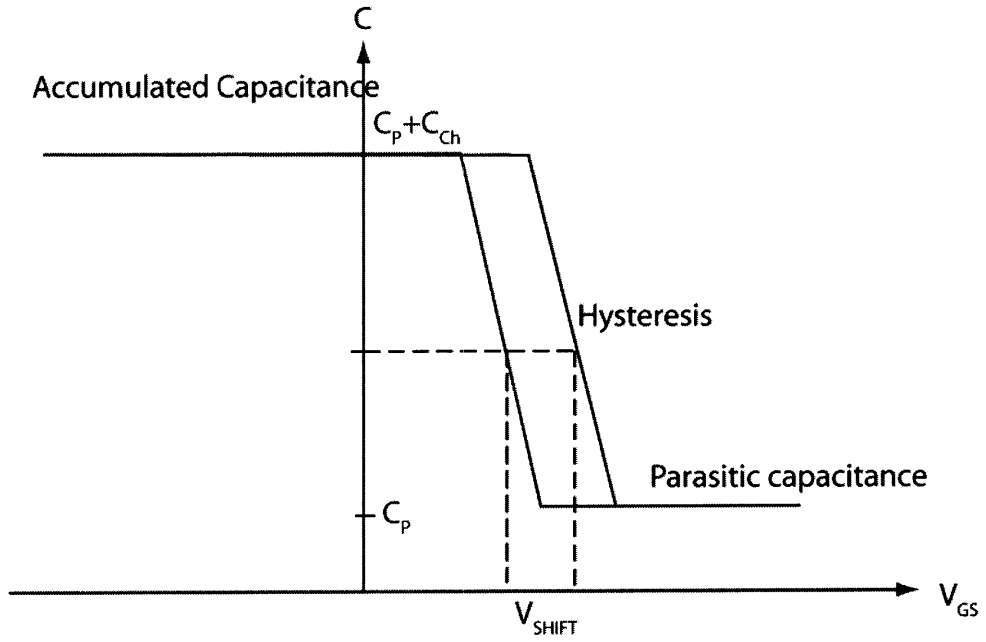

Figure B-4. C-V plot. Hysteresis can be measured by V_{SHIFT}.

3.9 Contact Resistance ($R_{CONTACT}$)

Due to the metal-semiconductor junction at the source and drain end, there are Schottky-diodes that act like injection barriers at the contacts. The injection barriers lead to contact resistance, and it can be extracted out using the linear region transfer characteristics described in Section 2.2, and it is dependent on the gate voltage. It can be used to predict device performance by length scaling. It is measured by plotting V_{SD}/I_{SD} vs. channel length. At the linear extrapolation at length = 0 is the contact resistance. To compare the performance of different transistors, a single value is picked, and for now V_{SG} = 20 V is picked arbitrarily.

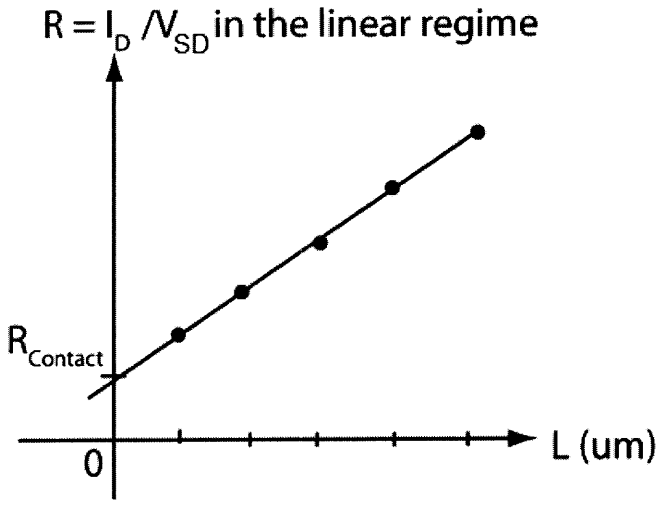

Figure B-5. Extraction of the contact resistance.

3.10 Mobility (μ)

The mobility can be extracted by the simple relationship, $I_{SD} = (W/L)\mu Q V_{SD}$. Q is a function of V_{SG} and can be derived by integrating C-V plots with respect to V_{SG}. Since the relationship only applies in the linear region, and is severely affected by contact resistance, the effect of the contact resistance must be cancelled out. The mobility increases as the gate voltage increases. For comparison, a single value is picked at $V_{SG} = 20V$.

4. Length Considerations

In order to compare technologies, the shortest transistors with the given technology should be measured and characterized. However, in order to compare the quality of the semiconductor itself, it is beneficial to compare the transistor with sufficient length because the short transistors' performance has a tendency to be dominated by the contact regions where there is a high non-linear contact resistance. For this reason the characterization is done in two different lengths: 5 μm and 25 μm, which is the shortest and the longest channel lengths in our current mask set, respectively.

5. Table of measured parameters

Parameter	Mean	Std. Dev.	Maximum	Minimum
$I_{G,leak}$ [fA/μm]	17	22	70	<1
$I_{DS,leak}$ [fA/μm]	1.2	0.89	2.1	<1
S [V/dec]	0.64	0.21	1.1	0.34
V_T [V]	0	1.5	3	-2
on/off Ratio	9.7E+07	1.2E+08	3.3E+08	2.9E+06
I_{ON} [nA/μm]	11	8.8	29	3.3
C_P [fF/μm]	4.4	1.0	5.9	2.8
C_{Ch} [nF/cm^2]	24	3.8	28	17
V_{SHIFT} [V]	0.19	0.17	0.40	0
$R_{CONTACT}$ [MΩum]	6.0E+02	3.6E+02	1.4E+03	8.2E+01
μ [cm^2/Vs]	0.030	0.015	0.062	0.012

Table B-1. Compiled OTFT parameters from seven most recent wafers.

Appendix C MATLAB Code for DOS Extraction

```
function [tau, a, c, r] = fit_tau6(t, mData, range, doPlot, saveFilename)

% fit_tau6 fits mData with np (=80) exponential decay
% Optimization function written by Jungwoo Joh.
% Modified by Kevin Ryu.
% t = time data
% mData = measured data
% range = [1 1e5] -> range of data to look at.
% doPlot = 2
% saveFilename = 'filename'

from = 1;
to = length(t);
for k = 1:length(t)-1
    if t(k) <= range(1) & t(k+1) >= range(1)
        from = k+1;
    end
    if t(k) <= range(2) & t(k+1) >= range(2)
        to = k+1;
    end
end

t1 = t(from:to);
i1 = mData(from:to);
d_mData = mData(from)-mData(to);
d2 = (max(i1) - min(i1));

tau_l = 10^round(log10(t1(1))-0.5);
tau_u = 10^round(log10(t1(length(t1)))+ 1);

np = 80;
if length(t1) < np
    np = length(t1)-1;
end
tau = logspace(log10(tau_l), log10(tau_u), np);
b2 = 1./tau;
C = zeros(length(t1), np + 1);
C2 = zeros(np + 1, np + 1);
C3 = zeros(np + 1, np + 1);
D = zeros(length(t1), 1);

for j = 1:length(t1)
    for k = 1:(np + 1)
        if k < np + 1
            C(j, k) = exp(-b2(k)*t1(j));
        else
            C(j, k) = 0; % last term is for constants modified to 0 from 1
        end
    end
    D(j, 1) = i1(j); % D is mdata
end
for j = 1:np
    if j < np
        C2(j, j) = 1;
        C2(j, j+1) = -1;
    end
```

```
    C3(j, j) = 1;  % C3 is I dim np but C3(np+1,np+1)=0;
end

x0 = [zeros(1,np) mData(to)+d2*0.05]';
lb = [zeros(1,np)-d2/2 mData(to)]';
ub = [zeros(1,np)+d2/2 mData(to)+d2]';
option6 = optimset('LargeScale', 'On', 'MaxIter', 5, 'TolFun', 1e-300);
option7 = optimset('LargeScale', 'On', 'MaxIter', 1, 'TolFun', 1e-300);

x = x0;
iter = 1;
I0 = 0;
for k = 1:length(t1)-1
    I0 = I0 + (i1(k)+i1(k+1))/2*(t1(k+1)-t1(k));
end
I1 = I0;
I1prev = -I1;
maxErr = 1;

s = sprintf('Starting new optimization....  I0 = %e, mean i1 = %e', I0,
mean(i1));
disp(s);
if doPlot > 1
    figure (200);
    figure (201);
end

while abs((I1prev-I1)/I1prev) > 0.01 | iter < 32 | doPlot > 1
    %only number of iterations in option6 is changed for each loop
    option6 = optimset('LargeScale', 'Off', 'MaxIter', iter, 'TolFun', …
      1e-300, 'Display', 'Off');
    [x fval ef] = fmincon(@(x)costFunction(x, D, C, C2, C3), x, [], …
      [], [], [], lb, ub, [], option6);
    f = C*x; %x is the extracted amplitude at various tau.
    res = (f - i1);
    maxErr = max(abs(res./i1));
    I1prev = I1;
    I1 = 0;
    for k = 1:length(t1)-1
        I1 = I1 + (abs(res(k))+abs(res(k+1)))/2*(t1(k+1)-t1(k));
    end
    iter = iter * 2;
    s = sprintf('I1/I0 = %e, maxErr = %e', I1/I0, maxErr);
    disp(s);
    if doPlot > 1
        figure (200);
        hold off;
        semilogx(t1, i1, 'ro');
        hold on;
        semilogx(t1, f);
        figure (201);
        semilogx(tau, x(1:length(x)-1));
        cont = input('Enter to continue...');
        if length(cont) ~= 0
            break;
        end
    end

    if ef ~= 0
        s = sprintf('Exit flag not zero (%d), so exit.', ef);
        disp(s);
        break;
    end
    if iter >= 512      %iter(ation) decides the accuracy.
```

```
        disp('Too many iterations. Just exit..');
        break;
    end
end

r = sqrt(mean((res./i1).^2));   % relative? rmse

a = x(1:length(x)-1);
c = x(length(x));

tl = round(log(tau_l));
th = round(log(tau_u));

if doPlot
    fs = 16;
    figure;
    set(gca, 'linewidth', 3);
    f = C*x;
    mul_con = 1;
    plot(t1, 1-mul_con*i1, 'ro');
    hold on;
    plot(t1, 1-mul_con*f', 'linewidth', 3);
    xlabel('Stress time (s)', 'fontsize', fs);
    ylabel('\Delta V/\Delta V _{FINAL}', 'fontsize', fs);
    title_s=sprintf('Relative rmse=%e', r);
    %title(title_s, 'fontsize', 13);
    set(gca,'FontSize',fs, 'xscale', 'log');
    xlim([tau_l tau_u]);
    set(gca, 'xtick', logspace(tl, th, th-tl + 1), 'xminortick','off');
    if i1(1) < 0
        %set(gca, 'ydir', 'reverse');
    end

    if nargin >= 5
        saveas(gcf, [saveFilename '_raw.fig']);
    end

    figure;
    semilogy(a , tau, '.-');
    hold on;
    plot(0*tau, tau, 'k-');
    ylabel('\tau_{trap} (sec)', 'fontsize', fs);
    xlabel('DOS (N_T)', 'fontsize', fs);
    title_s=sprintf('Relative rmse=%e', r);
    %title(title_s, 'fontsize', 13);
    set(gca,'FontSize',fs, 'yscale', 'log');
    ylim([tau_l tau_u])
    set(gca, 'ytick', logspace(tl, th, th-tl + 1), 'xminortick','off');
    p = get(gcf, 'position');
    p = p + [0 -450 100 0];
    set(gcf, 'position', p);
    if i1(1) < 0
        %set(gca, 'ydir', 'reverse');
    end

    if nargin >= 5
        saveas(gcf, [saveFilename '_tau.fig']);
    end
end
```

```
function cost = costFunction(x, Y, A, B, C)

% costfunction for fit_tau6 optimization function
% Originally written by Jungwoo Joh.
% Modified by Kevin Ryu.
% y-A*x is the error
% B*x is the difference between adjacent fit parameters

cost = norm(Y-A*x) + norm(x) + 0.1*sum(abs(x)-x);
```